Building and testing a setup for heating and performing quantitative measurements of iron concentrations in silicon wafers for solar cells

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Date: 7-6-2013

Thesis assignment description

The goal of this thesis work is to design, build and test a setup allowing for quantitative measurements of iron concentration in silicon for solar cells. Research will have to be done to determine how the existing Photoluminescence Imaging Setup can be upgraded for such measurements. Furthermore the setup has to be equipped with a sample holder that enables the wafers to be heated for measurements at different temperatures. After implementing, these new features will have to be tested to see if they function according to the requirements.

Date: 4-6-2013

Signature student: Signature company supervisor:

Summary

This report is written to guide the reader step by step through the process of developing a heating stage and a iron mapping device for a photoluminescence setup, used to measure the lifetime of silicon wafers in solar cells. Subject specific terms will be explained throughout the report.

First, research has been done to determine how silicon wafers are produced, what influences their lifetimes, why does iron contamination occur in silicon and how does a photoluminescence setup work. After understanding these basics, the requirements for the desired implementations could be formulated. The strengths, weaknesses, opportunities and threats were analyzed by a SWOT analysis. Then several concepts were devised and afterwards judged by their different properties. There is decided to use a hot plate to make a heating stage and to research if the standard equipment of the PL-setup can be used to make iron maps.

After implementing the chosen concepts in the PL-setup, several tests were done to monitor the performance of the new features. The heating stage turned out to be a large improvement of the old hot plates that were used, especially in terms of homogeneity. Some further improvements of the accuracy can be made by using a vacuum pump to suck the silicon wafer to the hot plate surface. The laser in the PL-setup was found to be incapable for making iron maps, but further research and adjustments on the setup might give new opportunities. It is however determined that an external high intensity light source, in this case a flash head, can be used to replace the laser.

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Introduction

This report describes the process and results of my bachelor thesis for The Hague University in Delft. The work for this thesis is done at the solar department of the Institute for Energy Technology in Norway. The goal is to prove that all necessary competences of a mechanical engineer are gained and can be brought into practice. My thanks go out to everybody at IFE who helped me during this time. Special thanks go to Erik Stensrud Marstein from IFE and Frederik de Wit from The Hague University for supervising me.

1 Background

1.1 Norwegian Institute for Energy Technology

The Institute for Energy Technology (IFE) in Norway was founded in 1948 to do research on nuclear energy. Nowadays the field of research has been expended to energy, environmental technology, physics, material science, petroleum technology and nuclear safety and reliability. IFE owns and operates the only two nuclear reactors in Norway.

Figure 1: Institute for Energy Technology campus in Kjeller, Norway. (IFE Google Plus Images)

1.2 Solar department

This thesis will be carried out at the Solar Energy Department. IFE has been doing research on solar energy from the nineties and since 2008 the department for solar energy was founded. This department focuses on improving solar cells, in particular crystalline silicon cells since these are the ones mainly used in industries. According to IFE's website the research covers the following topics:

- Production of solar grade silicon
- Modelling of crystallisation
- Improvement of existing solar cell technology
- Development of new solar cell technology
- Solar cell characterization
- Investigation of the effect of material quality upon solar cell efficiency

All research is done in close contact with the Norwegian solar cell industry. The laboratory has a silicon solar cell production line. Additionally, a well-equipped characterization laboratory has been built up. (IFE Solar Energy)

2 Problem and assignment

2.1 Situation

Currently the BT imaging LIS-R1 photoluminescence setup (PL setup) is used to make calibrated lifetime images of silicon wafers. These images give information about the quality of the wafer and so in the end about the efficiency of the solar cell. For iron mapping the μ-PCD setup is used. This setup scans the wafer and produces an iron map, but to get a single high resolution image can take up to several hours. By using the PL setup this could be reduced to a few seconds.

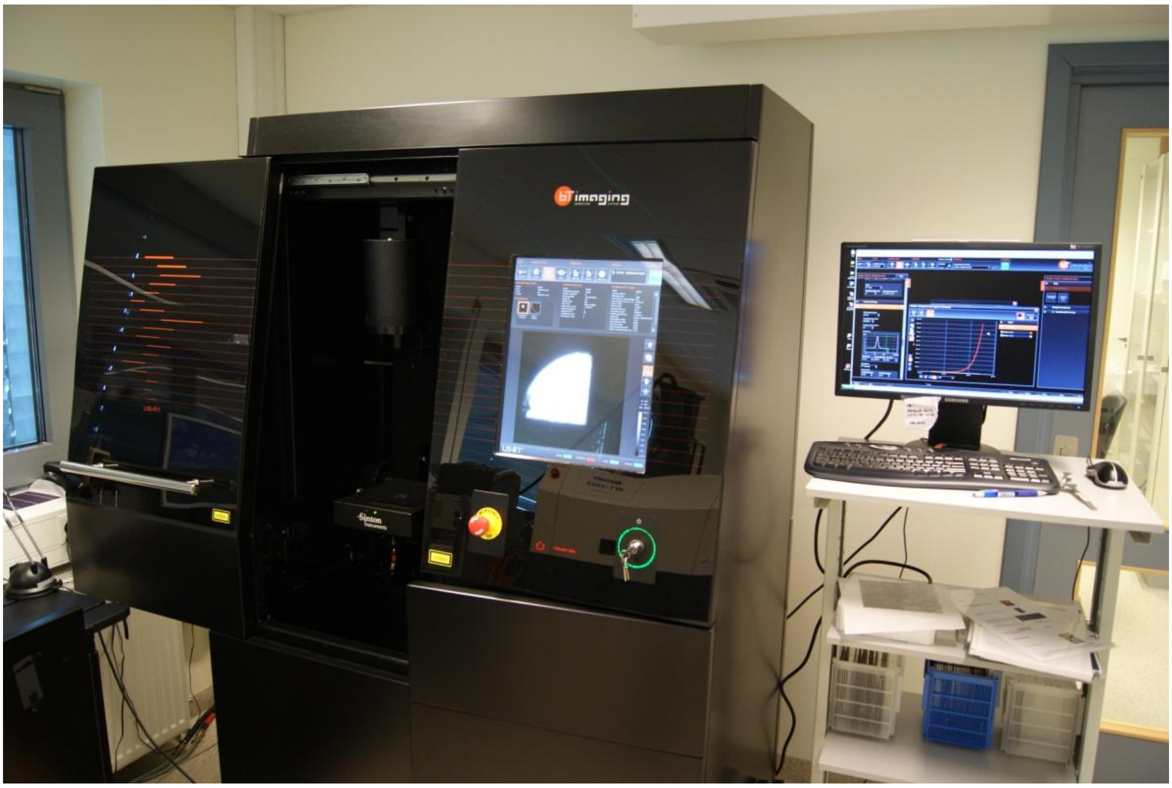


Figure 2: Photoluminescence setup

2.2 Problem

The PL-setup does not have the possibility to illuminate samples at an intensity high enough to split iron-boron pairs in silicon which is necessary to measure iron concentrations . The intensity that is required to do this is comparable with 10 times the intensity of sunlight (10 suns = 1 W/cm^2). More about iron-boron splitting will be explained in the next chapter. Furthermore, samples cannot be heated or cooled in the setup to do measurements at different temperatures.

2.3 Assignment

The goal of this thesis work is to design, build and test a setup allowing for quantitative measurements of iron concentration in silicon for solar cells. Research will have to be done to determine how the existing Photoluminescence Imaging setup can be upgraded for such measurements. Furthermore the setup has to be equipped with a sample holder that enables the wafers to be heated for measurements at different temperatures. After implementing, these new features will have to be tested to see if they function according to the requirements.

3 Basics of silicon wafers for solar cells

This chapter explains some basics to have a better understanding about how the photoluminescence setup works and why there are iron impurities in silicon wafers.

3.1 Multi-crystalline solar cell production

To understand how iron and other impurities enter in the multi-crystalline silicon wafers and to know when it can be detected, the entire production chain of a solar cell has to be taken into account . The production of the wafers is a process that has been researched for the last decades to improve the efficiency and at the same time lower the costs.

1. Ingot production
There are several techniques to produce the silicon blocks, but most used is casting. First the silicon is melted, then the heat is slowly extracted making the silicon to crystallise. This crystallization results in a inhomogeneous distribution of the wafer characteristics. During casting iron impurities enter the silicon from the crucible, the furnace and the coatings. These impurities segregate due to the high temperatures and so distribute trough the silicon. The result is that the top section of the ingot, that crystallizes first, is being cleaned because the impurities are being ´pushed´ away to the lower and side sections. Therefore the lower sections will show a higher impurity grade also due to close contact to the crucible walls, resulting in a lower efficiency. (Schönecker, Geerligs, & Müller, 2003)

2. Wafer grinding and slicing
After its production the ingot has to be grinded to get squared blocks. These blocks are sliced by saw wires, producing wafers. Nowadays the wafer thickness varies between approximately 150-250 μm.

The image below shows two steps described above:

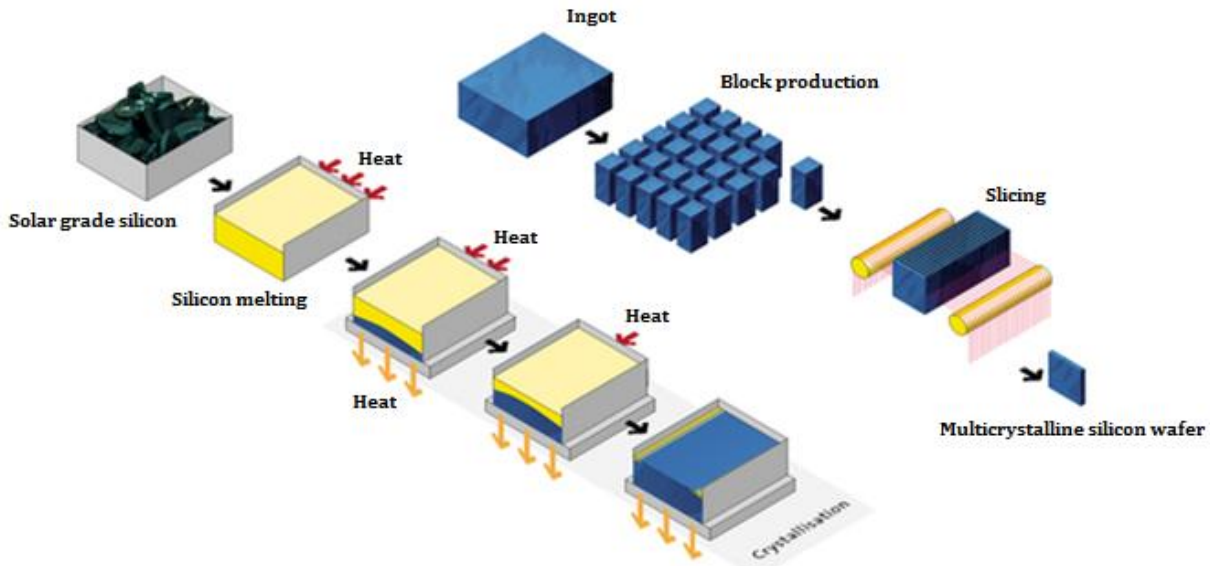


Figure 3: From solar grade silicon to multi-crystalline silicon wafer (Marstein, Silicon Solar Production, 2012)

3. Wafer cleaning
The wafer surfaces are washed. After the production in the factory, the wafers usually get some additional treatments in the solar cell factories, listed below:

4. Damage removal

Alkaline or acidic etches are used to remove damaged and contaminated surface layer. This is done in a so called wet bench. Typically 5 to 10 µm are removed from both sides.

Figure 4: Surface after damage removal. From left to right: the wet bench, the silicon surface, the silicon surface schematically and an image of the grain boundaries. (Marstein, Silicon Solar Production, 2012)

5. Texturing

To get a high efficiency out of the solar cell it is important to absorb as much sunlight as possible. Therefore a texturing process is performed to minimize reflectance. Again alkaline and acidic etches are used to remove a few µm on both sides.

Figure 5: Surface after texturing. From left to right: the wet bench, the silicon surface, the silicon surface schematically and an image of the grain boundaries. (Marstein, Silicon Solar Production, 2012)

6. Emitter diffusion

The emitter is added to supply the required charge separation. This is usually done by diffusion of $POCl_3$ gas. There are several techniques such as: spraying, spinning, mist evaporation and screen-printing possible to do this. During this process also gettering occurs. This is a process where metallic impurities are trapped in less critical sites and so eventually reducing their impact on the efficiency.

Figure 6: Surface after diffusion. From left to right: adding emitter, the silicon surface and the silicon surface schematically. (Marstein, Silicon Solar Production, 2012)

7. Edge isolation

During the previous diffusion step some of the phosphor evaporates and diffuses to the sides and rear of the wafer. This can create "shunts" (short-circuits). To solve this problem the wafer can be plasma or wet etched after the diffusion.

Figure 7: Surface after edge isolation. From left to right: the silicon surface and the silicon surface schematically. (Marstein, Silicon Solar Production, 2012)

8. ARC deposition

The next step is to add an anti-reflection coating of silicon nitride that doesn't affect the solar cell characteristics.

Figure 8: Surface after ARC deposition. From left to right: the surface of the solar cell and the surface schematically. (Marstein, Silicon Solar Production, 2012)

9. Contact formation

Finally metal contacts are made on both sides of the solar cell. This is done by screen-printing and metal pastes are dried in an oven. The front side pattern is always a compromise between shading and resistive losses.

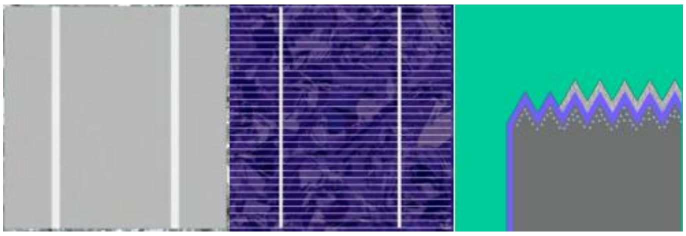


Figure 9: Surface after screen-printing. From left to right: backside of the solar cell, front side of the soloar cell and the surface schematically. (Marstein, Silicon Solar Production, 2012)

3.2 Solar cell operation

After the steps described in the previous paragraph the result is a multi-crystalline solar cell. Figure 10 shows a schematic image of such a solar cell.

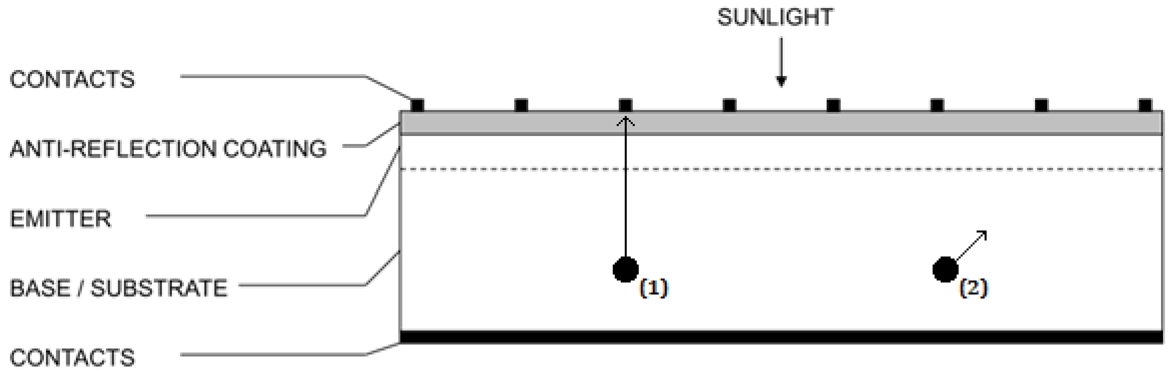


Figure 10: Intersection silicon solar cell (Marstein, Silicon Solar Production, 2012)

When sunlight reaches the silicon material in the solar cell it generates either electron-hole pairs or excitations, depending on what doping is used. In figure 10 two excited electrons are showed. After excitation electrons start moving around. The time it takes before an electron to stop moving and recombine is called minority carrier lifetime. In order for a solar cell to produce electricity, an electron needs to reach the contacts on the outside of the cell which are connected to a external circuit. So the longer the lifetime of the electrons, the bigger the chance they will reach a contact. This means that with a long lifetime (electron 1 in Figure 10) there are more electrons reaching the contacts, so more electricity is generated. Electron 2 however shows what happens if the lifetime is short. The electron recombines before it reaches one of the contacts and therefore no electricity is generated. In short, high lifetimes means a high solar cell efficiency and low lifetimes means a low efficiency.

Impurities in the silicon make it more difficult for electrons to move to the sides and therefore lower the lifetime.

3.3 Photoluminescence basics

Photoluminescence is a non-contact testing method to map minority carrier lifetime and detect micro cracks and defects in as-cut and semi-processed wafers. In this thesis photoluminescence technique(PL) will be used to detect iron impurities in multi-crystalline silicon wafer. Since it is an optical technique it is non-destructive and there is little need of sample manipulation or environmental control. Furthermore it is proven to be a fast measuring method. The identification of impurities and defects depends on their optical activity and is therefore not usable for the detection of every kind of impurity. Nevertheless it is a suitable method to find iron.

Photoluminescence can be explained as following: when light with enough energy reaches a certain material, the photons are absorbed and electronic excitations are created. Eventually these excitations relax and the electrons return to ground state (recombination) sending out light. This emitted light can be measured and analyzed. The intensity gives a measure of the relative rates of recombination. The time it takes the electrons to return to ground state is called the carrier lifetime, this is important for making lifetime images and will be explained later.

Variation of the PL intensity with external parameters such as temperature and applied voltage can be used to characterize the underlying electronic states and bands. With short laser pulses exited populations of electrons can be produced, the PL signal they emit can be monitored to determine recombination. (Gfroerer, 2000)

The image below shows the instrumentation that is usually present in a PL-setup. A laser illuminates the sample, hence by photoluminescence the sample will emit light. This light is detected by a camera. The intensity and photon flux of the light can then be analyzed. The photon flux is the amount of photons per second per square centimeter [s/cm^2].

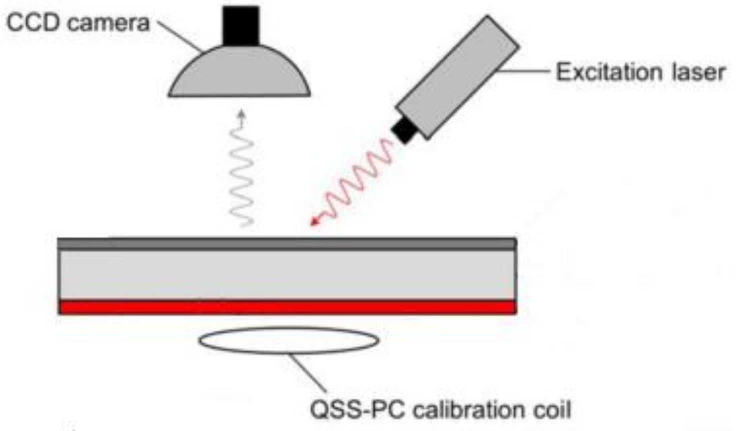


Figure 11: Typical photoluminescence setup (Haug)

The picture below shows the PL-setup used at IFE.

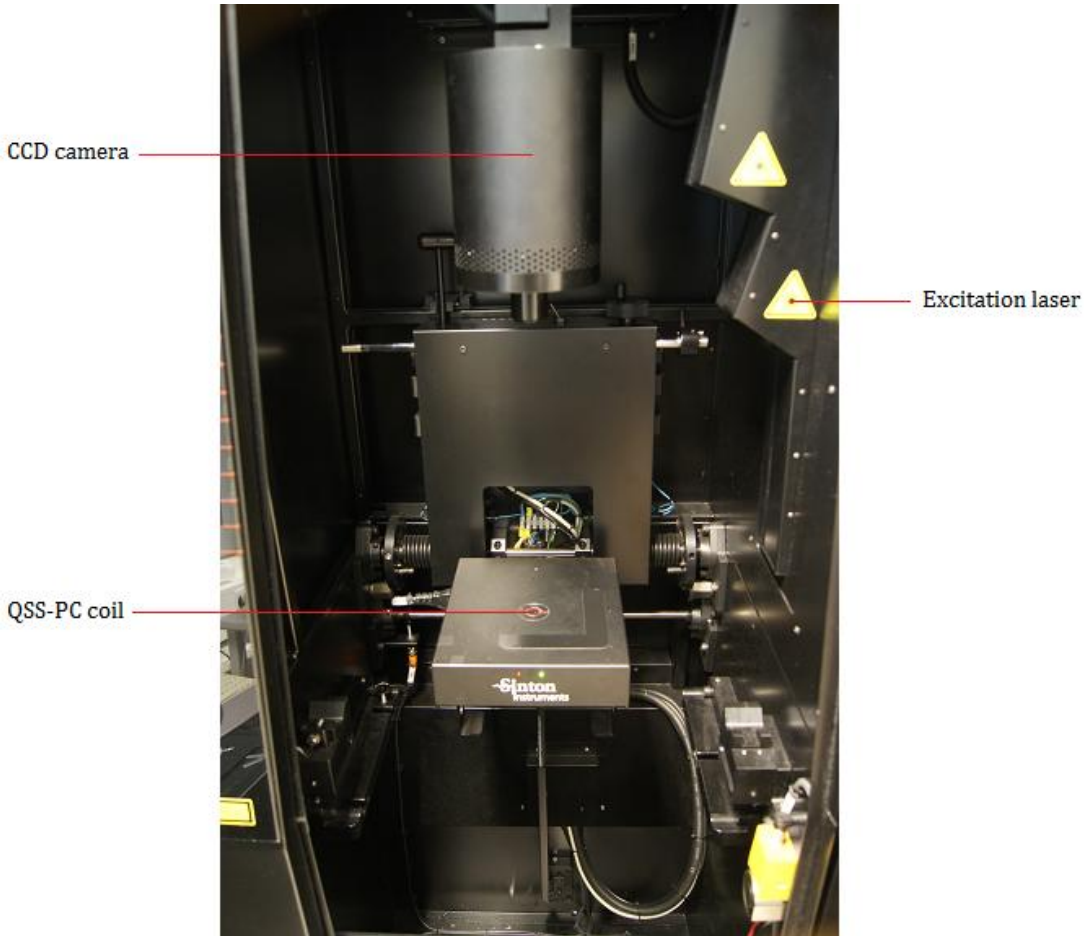


Figure 12: Laser, camera and coil in PL setup used at IFE

3.4 Quasi-steady-state photoconductance technique

Quasi-steady-state photo conductance (QSS-PC) is the technique used to generate calibrated lifetime images of the silicon wafers. Quasi-steady-state (QSS) means the illumination intensity declines slowly to zero. The decline should be long enough to ensure the recombination process. The conductivity is measured by a coil in the stage. This method using photoluminescence has proved to be excellent for measuring carrier lifetimes. A high conductivity means that many electrons have reached the surface of the silicon and so the carrier lifetimes are high. (Rein, 2004)

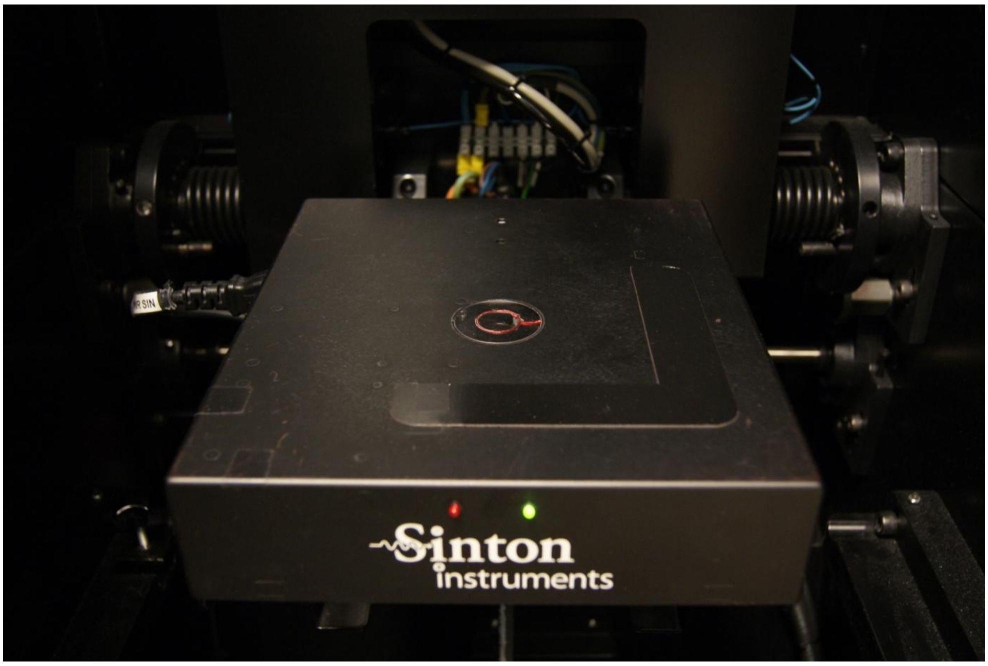


Figure 13: Calibration stage with coil in the middle

Figure 14 shows an example of a QSSPC measurement. It shows the dependency of the lifetime from the injection level. The y-axis gives the effective lifetime in seconds and the x-axis the injection level in photons per cubic centimeter.

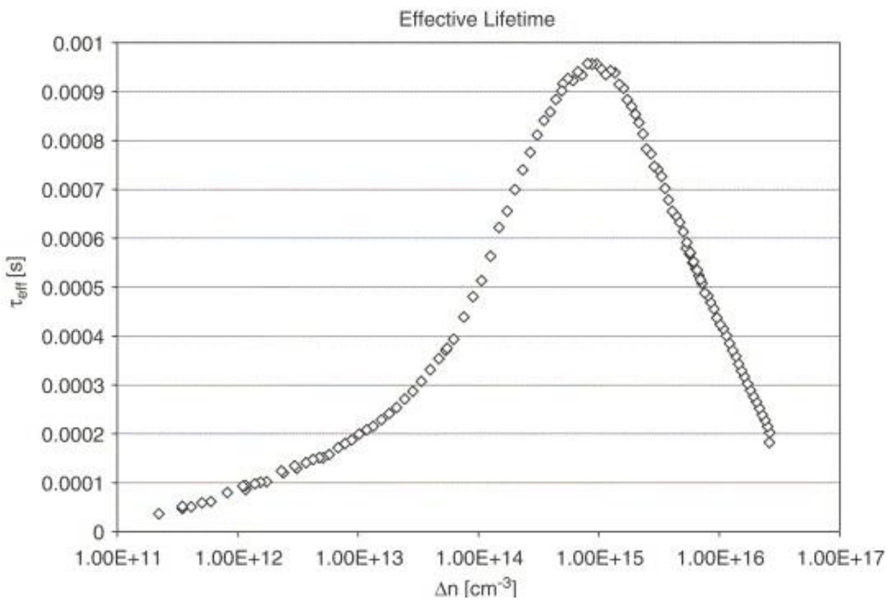


Figure 14: Injection dependent lifetime measurement with QSSPC method. (Agostinelli, 2006)

3.5 Iron mapping

During the production of the wafers described in chapter 2.1 impurities arise in the wafers. In this thesis there will be a focus on measuring the iron impurities which are present in the form of interstitial iron (Fe_i) or iron-boron pairs (FeB). Under illumination FeB pairs can split in Fe_i which changes the carrier lifetime significantly and so this change can be used to measure the amount of iron by monitoring the lifetime before and after splitting. The illumination intensity needed to split the FeB pairs is around 1 [W/cm^2] which is the equivalent of approximately 10 suns.

However, one condition is that iron defects must be dominating. Since there are many defects that can play a role so it is important to determine if iron is the lifetime deciding defect.

$$\frac{1}{\tau} = \frac{1}{\tau_{FeB}} + \frac{1}{\tau_{lid}}$$

This formula, in which τ is *lifetime* and *lid* stands for *light induced degradation*, shows that lifetime is influenced by all defects. To find out if FeB is lifetime deciding, the so called *cross over point* had to be determined. When a QSS-PC lifetime curve is made before and after the 10 sun illumination, than these curves are supposed to cross somewhere in the region of an injection level of 10^{14}-10^{15} photons per cm^3.

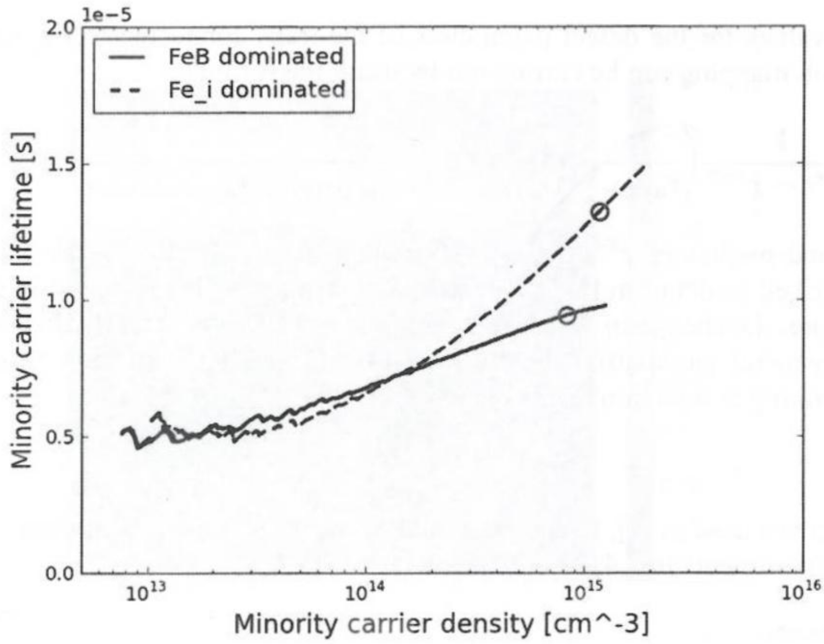


Figure 15: Cross over point (Angelskar, 2011)

When using photoluminescence to do iron mapping the injection level is determined in each point of the image. The iron concentration is than given by the following formula:

$$[Fe_i] = \frac{1}{X^{Fe_i} - X^{FeB}} \left(\frac{1}{\tau_{after}} - \frac{1}{\tau_{before}} + \frac{1}{\tau_{Auger,after}} - \frac{1}{\tau_{Auger,before}} \right)$$

Both the lifetime (τ) and the prefactors X^{Fe_i} and X^{FeB} depend on the injection level. Also the doping level is included in the prefactors.

4 Analysis and requirements

This chapter describes the requirements that the setup must fulfill after implementing the upgrades. If these requirements are met, the PL setup should enable scientists at IFE to do research in new areas of silicon wafers. Additionally function analysis of heating and illuminating the wafers are given. Finally a SWOT analysis is made to get an insight about the strengths, weaknesses, opportunities and threats of upgrading the setup.

4.1 Set of requirements

The setup has to fulfill the following requirements:

- Ability to heat sample with a temperature range between 20-200 [°C]
- Homogeneous heating of the sample [+/- 1,0 °C]
- Stage conductivity must be as low as possible
- Ability to illuminate sample with intensity of approximately 10 suns [1 W/cm^2]
- Minimize influence from stage on measurements
- New stage has to be easy to remove
- PL-setup must have as less down-time as possible

4.2 Function analysis heating wafers

To make an image of a heated wafer using the PL setup without the new stage requires the procedure shown in Figure 16: Procedure for imaging heated wafers before new stage . It is a time consuming procedure, because the wafer has to be removed and heated again for every set point. Furthermore the data will be unreliable because the wafer will cool down rapidly after being removed from the hot plate and placed on the calibration stage. Finally the hot plate is expected to heat the wafers not homogeneously, which can make the results useless. Therefore goal is to simplify and improve the steps that are shown in dark blue.

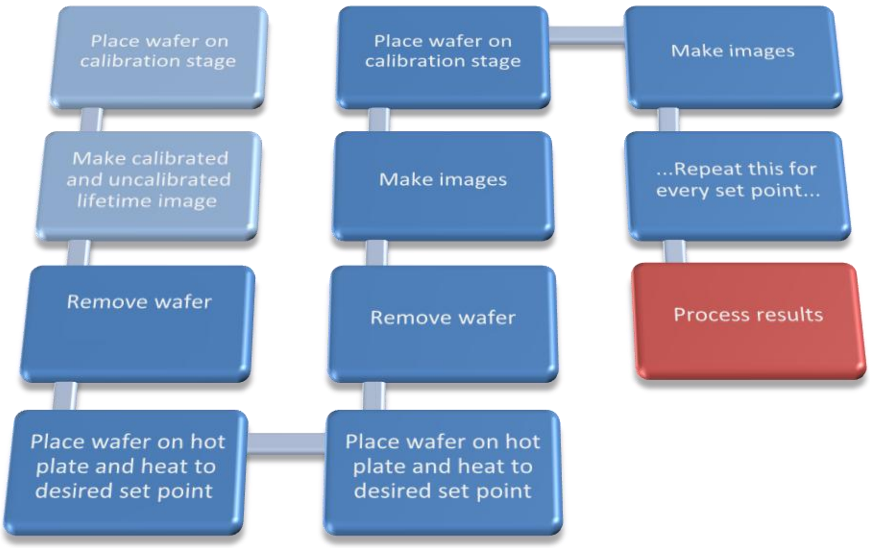


Figure 16: Procedure for imaging heated wafers before new stage

4.3 Function analysis high intensity illumination of wafers

Currently there are no iron maps made by using the PL-setup at IFE. However there is a way in which it should be possible to do so. Figure 17 shows this procedure. The goal is to make iron maps by using only the PL-setup, so that the wafers don't need to be taken out during the measurements. The steps in dark blue will be improved and simplified.

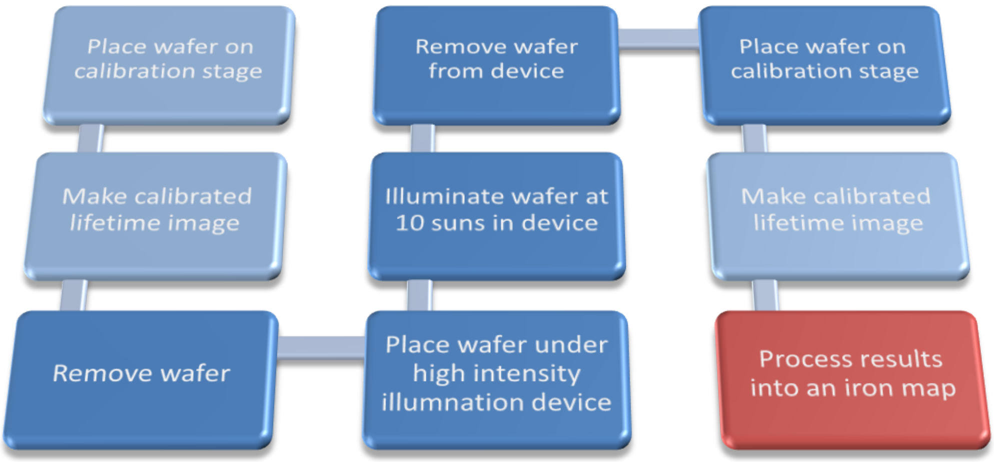


Figure 17: Procedure for high intensity illumination

4.4 SWOT analysis

A SWOT analysis has been made on implementing iron mapping and a heating feature in the PL-setup. This analysis focuses on the strong and weak points and gives an overview of the opportunities and threats.

Strengths	**Weaknesses**
- Non destructive - No sample manipulation - No environment control - Fast imaging technique	- Currently no possibility for iron-boron pair Splitting in the PL - Stage cannot be heated
Opportunities	**Threats**
- Space in setup for additional components - Laser can be focused on small area too reach high intensity levels - Stages are removable	- Complicated software adjustments - Overheating problems with use of high intensity lights - New stage cannot do calibration - New stage needs to be on exactly same height as calibration stage - Costs - Maybe not a must have for industries

Table 1: SWOT analysis

5 Concepts

Since the two new features that will be developed, heating and illumination, are not directly linked in terms of functionality or design requirements, it is possible to make separate concepts and combine the best options for both features. Concepts are made for both heating and illumination silicon wafers and shown in following tables.

5.1 Concepts for heating wafers in PL-setup

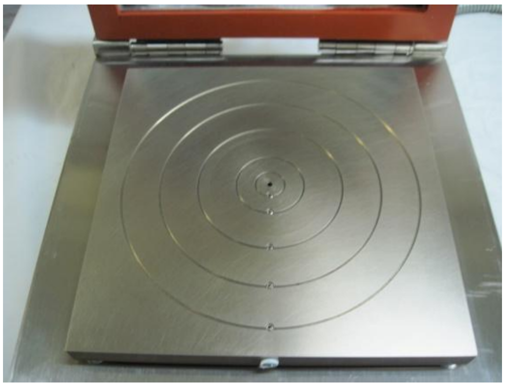
Concept 1 **Hot plates**	- Temperature range 49-375°C - Temperature controlled by digital thermostat - Accuracy: 1% of set point - Surface flatness: 0,1 mm - Vacuum channels for optimal contact between wafer and plate giving a homogenous temperature deviation	
Concept 2 **Industrial blower**	- Temperature up to 60°C - External temperature measurement of wafer required - Difficult to heat wafers homogenously - Low accuracy	
Concept 3 **Infrared heater**	- Temperature range up to 700°C - Recommended distance 100-200mm - Difficult to build in setup because shortage of space	
Concept 4 **Industrial batch oven**	- Temperature range up to 425°C - Homogenous heating possible - Cannot be build in, so wafers have to be placed into PL-setup after heating - No heating up of parts inside PL-setup	

Table 2: Concepts for heating wafers

The 4 concepts that are looked into to heat the wafers can be judged in a trade-off table. In this table every concept is valued by temperature homogeneity, accuracy, functionality and feasibility. The concept that scores best for a criteria receives a 4 and the one that scores worst receives a 1. The number in brackets behind these criteria stand for the weighting factor. This factor is used because some criteria are thought of to be more important than others.

	Temperature homogenity (3)	Accuracy (2)	Functionality (1)	Feasibility (2)	**Total score**
Hot plate	4	4	2	3	**28**
Hot air	1	1	3	4	**16**
Radiation	3	2	4	2	**21**
Oven/microwave	2	3	1	1	**15**

Table 3: Trade-off table heating concepts

From this table can be concluded that the hot plate concepts are the best solution to heat up wafers in the PL-setup. This concept will be worked out in more detail in the following chapter.

5.2 Concepts for iron-boron splitting in PL-setup

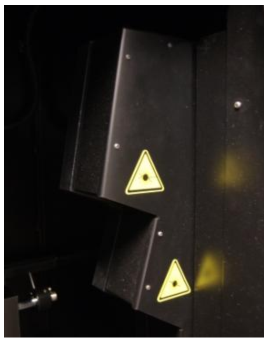
Concept 6 **Build-in flash head**	- 650W flash light - Output: 3000J - Dimensions: 19x12x16 cm - Intense heat production can be a problem inside the setup	
Concept 7 **Focussing existing laser**	- By focusing existing laser 10 suns intensity can be reached - Only software adjustments needed - Laser intensity: When focused the photon flux is 4,23*10^{18} cm^{-2} s^{-1} - No over-heating problems in setup	

Table 4: Concepts for illuminating wafers

Because there are only 2 concepts for iron-boron splitting no trade-off table will be made. Concept 7 will be tested first because no hardware changes have to be made and no parts have to be ordered. Concept 6 will be further developed if concept 7 turns out to be not effective.

5.3 Chosen concepts

By the use of the trade off tables and after discussing with experienced users of the PL-setup there is decided to combine concept 1 and concept 7 for a complete solution. This means that hot plates will be build in the setup. The existing laser will be tested to see if it is possible to split the iron-boron pairs in the silicon wafers, hence making the PL-setup suitable for iron mapping.

6 Implementation of chosen concepts

The hot plates were found to be the best solution to heat up wafers inside the PL-setup. The following paragraphs give more information about the chosen hot plate and how to implement them in the setup

6.1 Wenesco's HP66V hot plate

After a market research (see attachment I) the hot plates from Wenesco in Chicago, United States are found to satisfy the requirements best. This manufacturer makes standard hot plates developed for heating wafers. Other manufacturers have only standard equipment for heating larger items or heating up to higher temperatures. To customize a hotplate is financially not desirable.

The image below shows the hot plate that will be build into the PL-setup. It consists of three vacuum channels to make sure that the wafer makes excellent contact with the hot plate. This ensures that the temperature is homogeneously transferred. In the following paragraphs the specifications and integrated design are described.

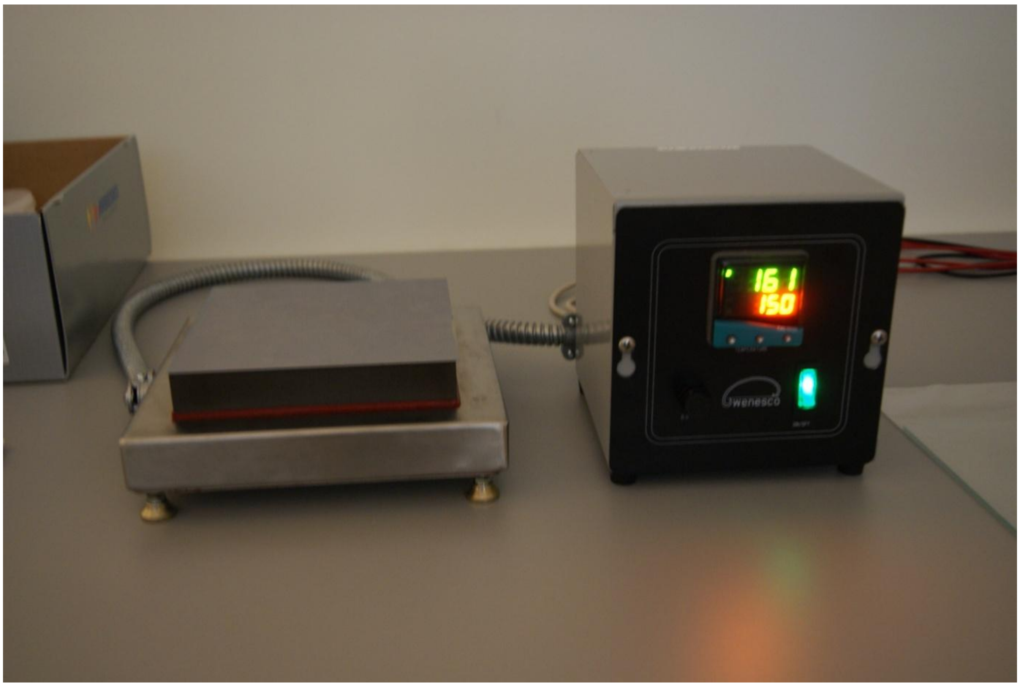


Figure 18: Wenesco HP66V hot plate

6.1.1 Specifications

The hot plate has the following specifications:

- Heated area: 15,24 x 15,24 cm
- Plate dimensions 15,24 x 15,24 x 2,54 cm
- The surface flatness to 0,0127 cm
- Plate material: anodized aluminum
- Plate type: 6 inch with PV3 vacuum ring pattern.

- Housing material: stainless steel
- Includes valves for vacuum supply
- An on-off valve is furnished for your vacuum supply
- Overall size is 20,32 x 20,32 x 10,16 cm
- Temperature controlled with digital thermostat accuracy: 1% of set point. Actual temperature and set points are digitally displayed.
- Temperature range: 49-375°C
- Voltage: 240 V
- Power: 1100 W
- Current: 4.58 A

6.1.2 Implementation

The hot plate needs to be integrated in the PL-setup. One of the requirements is that the heated stage can be easily removed after measuring. For this reason there is chosen to only use parts that do not have to be mounted permanently.

First of all the calibrated stage can be turned away so there is enough space in the PL. The power supply with digital controller can be placed on the bottom of the setup, because the power cables to the hot plate are long enough. Then a ground plate has to be placed in the pre-manufactured incisions in the side of the PL-setup. On this ground plate a adjustable support has to be placed. It is important that the heating stage is placed on approximately the same height as the calibration stage used to be, because the CCD camera is focused on this height. Finally the hot plate can be placed on the support.

To be able to make uncalibrated images some settings have to be changed. In default wafer setting the PL-setup is programmed to use the calibrated stage. However if this stage is turned away an error will be given. The settings have to be changed to 'block' measurements. The PL-setup knows that the calibration stage is not used, because blocks cannot be placed on this stage. With this settings the setup will allow to make uncalibrated images of the heated wafers.

The image below shows how the heat stage is can be placed in the PL-setup. This way the camera and laser don't need to be focused again and the stage can be removed easily.

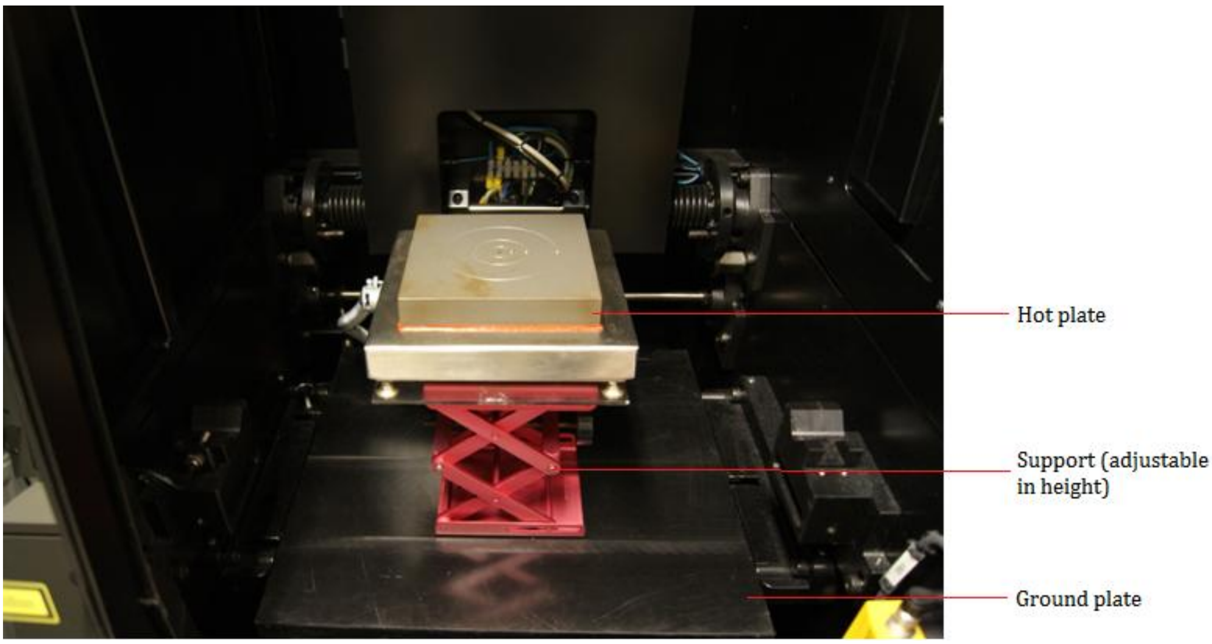


Figure 19: The hot plate integrated in the PL-setup

Figure 20 shows a wafer placed on the heated stage during heat measurements. It is recommended to use a infrared thermo camera to monitor the real temperature of the wafer. This camera will also be used during the tests in chapter 7.

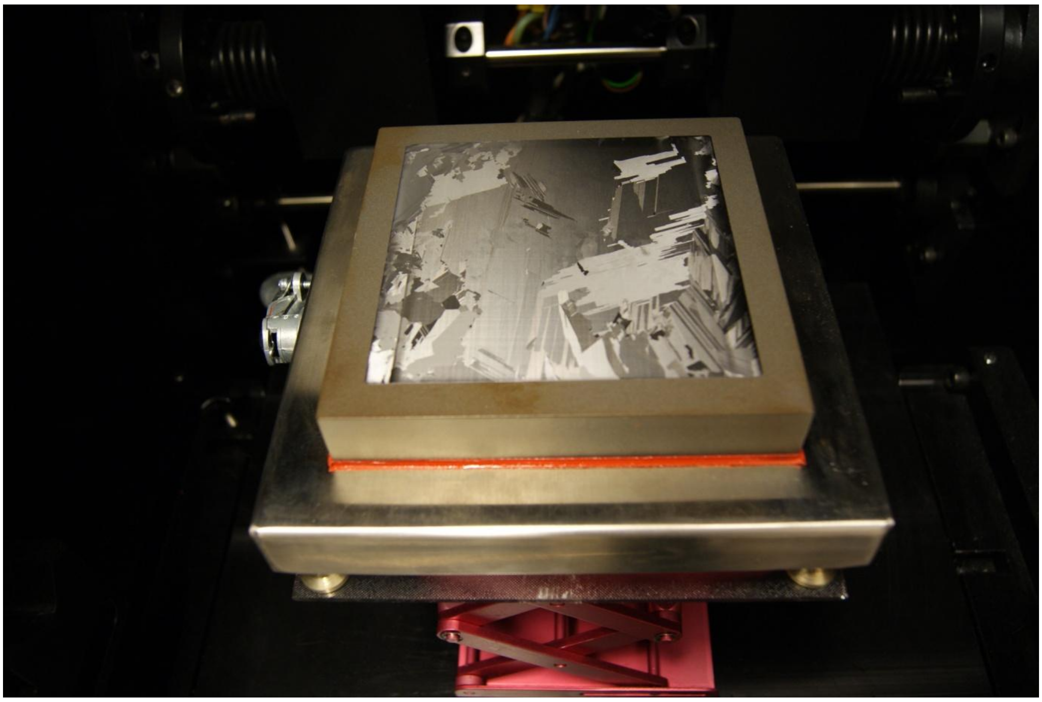


Figure 20: Wafer placed on heated stage during heat measurements

6.1 PL –laser

The high intensity illumination that is performed to split iron-boron pairs can be done by an external light source. However the PL-setup already contains of a laser that can reach intensity levels that should be high enough by focusing the laser. To save costs, it is examined if it is possible to make iron maps by using the laser. Another reason is that the PL-setup is used for many research projects at the same time. To build in another light source the entire setup will be out of use for a few days or possibly weeks. This could be unfavorable to the progress of other running projects.

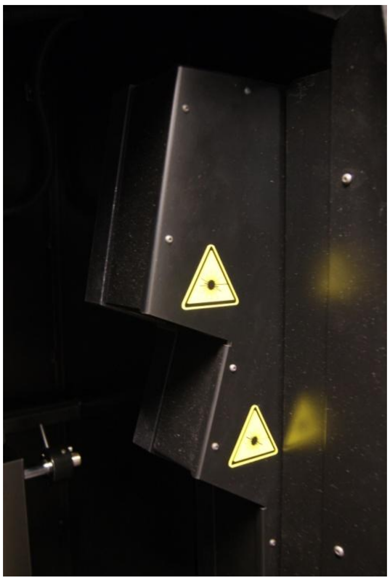


Figure 21: Laser in the PL-setup

7 Tests

This chapter describes several tests which are performed to find out if the new features of the PL-setup fulfill the requirements. Test 1, 2 and 3 are about iron mapping in the PL. Test 4 and 5 are done to monitor the performance of the heating stage. After every test a conclusion is drawn. An overall conclusion and recommendations will be given in chapter 8.

7.1 Test 1 – Finding cross-over point with PL laser; batch 1

Introduction
The first tests are performed on a set of old wafers with presumably a large amount of iron contamination. Previous research states that the wafer should be exposes to light with an intensity of 10 suns for 2 minutes to split the FeB pairs. (Angelskar, 2011)

Before and after this illumination a QSS-PC lifetime curve should be made of the wafer. If the curves have a cross-over point around a minor carrier density of 10^{14} cm^{-3} than it can be assumed that iron is a lifetime determining defect and that all the FeB pairs are split in interstitial iron (Fe_i).

Samples
The following specifications were given:

- Multi-crystalline silicon wafers
- Doping: p-type
- Thickness: 190μm
- Resistivity: 0,619
- Reflectivity: 20%

Procedure
The following steps has to be followed:

1. Place wafer on calibration stage
2. Make QSS-PC lifetime curve and calibrated image
3. Change laser settings to; illumination area: small
   illumination time: 30 s
   photon flux (intensity): 4,23* 10^{18} cm^{-2} s^{-1}
4. Make an uncalibrated image 4 times (4 x 30 s = 2min) with the previous laser settings. The image will be useless but the purpose of this step is to expose the wafer to 10 suns for 2 min.
5. Change laser settings back to default
6. Make a QSS-PC lifetime curve again and a calibrated image
7. Compare images before and after and determine if lifetimes have a cross-over point in the expected region (around injection level of $2*10^{14}$)

Results

In the following lifetime images the lighter the area the higher the lifetime in this place.

First wafer

The calibrated images below show the carrier lifetimes before and after 10 sun illumination. Dark areas are low lifetimes and the more light the higher the lifetime. We can see that lifetimes are very high in the lower left part of the wafer. It is visible in the images that the lifetime after illumination has dropped.

Before After

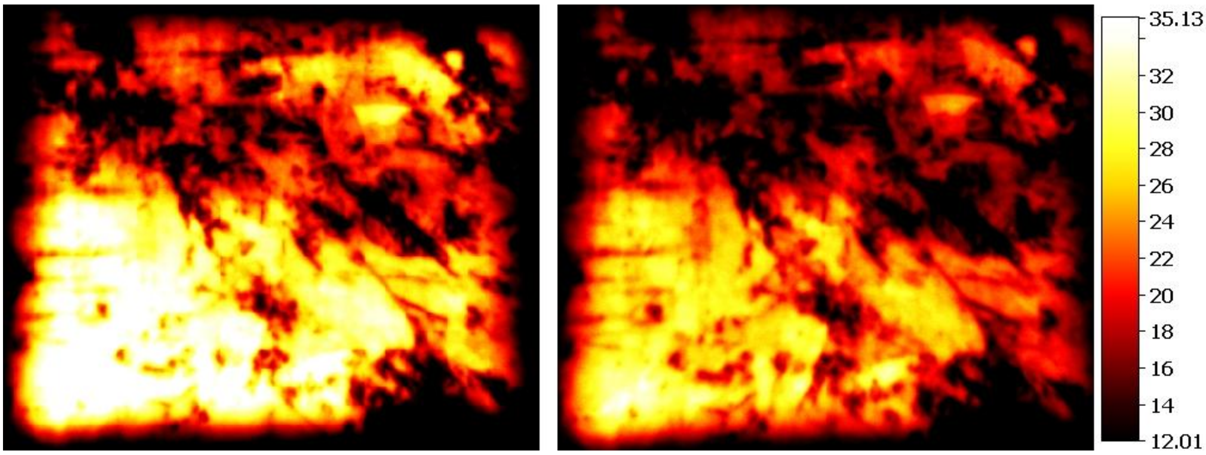


Figure 22: Calibrated images of wafer 1 before and after illuminating

The QSS-PC data gives the following values for the lifetime curves before and after. Δn is injection level in photons per cm^3, τ is the carier lifetime in seconds.

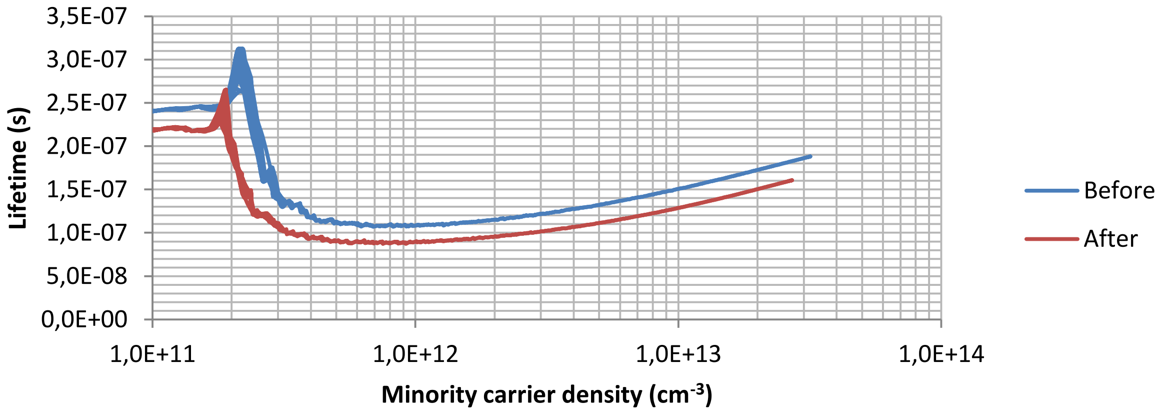


Figure 23: QSSPC before and after illumination of first wafer

The start of the curves in Figure 23 can be neglected, the unusual peak is because of trapping. We see there is no cross-over point. This means iron is not the dominant defect or the iron-boron pairs have not been split.

Second wafer
The second wafer has a high lifetime area in the right bottom part. It is visible that lifetime has decreased after illumination.

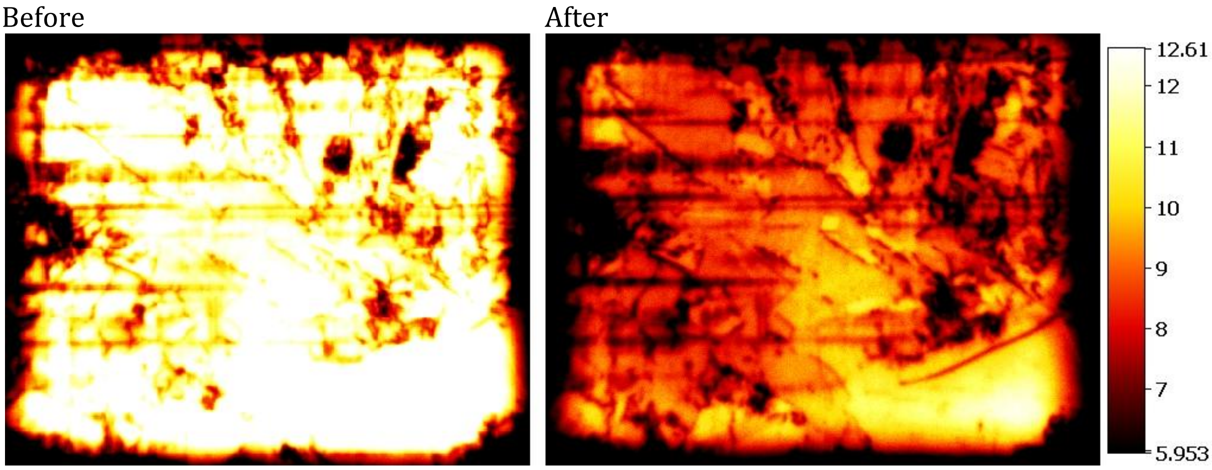


Figure 24: Calibrated images of wafer 2 before and after illuminating

The QSS-PC data gives the following values for the lifetime curves before and after. Δn is injection level in photons per cm^3, τ is the carier lifetime in seconds.

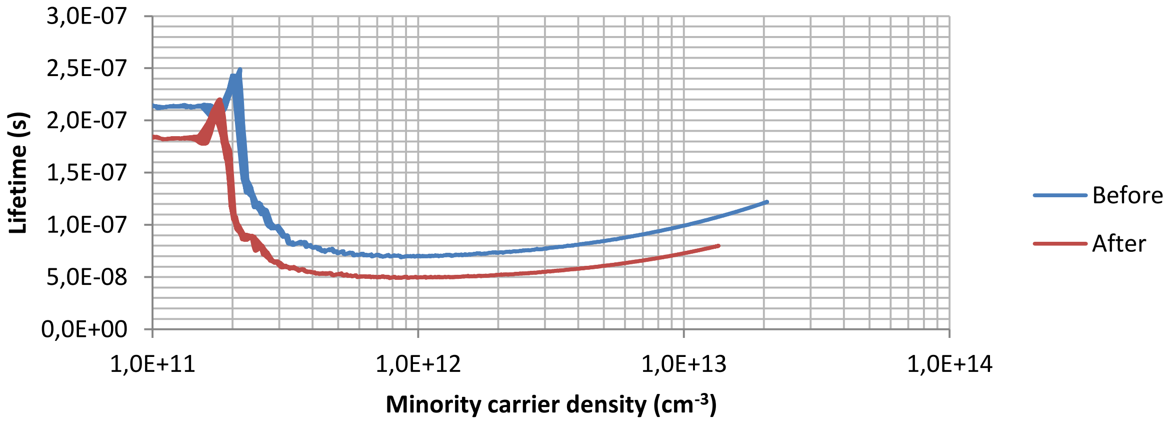


Figure 25: QSSPC before and after illumination of second wafer

The results of wafer 2 are very similar to wafer 1 so also here there are other defects more dominant or the iron-boron pairs are not split.

Third wafer

The third wafer seems to have a high lifetime throughout most of the wafer, but especially in the lower left part. The lower right part has low lifetimes and can be seen to have decreased after illumination.

Before After

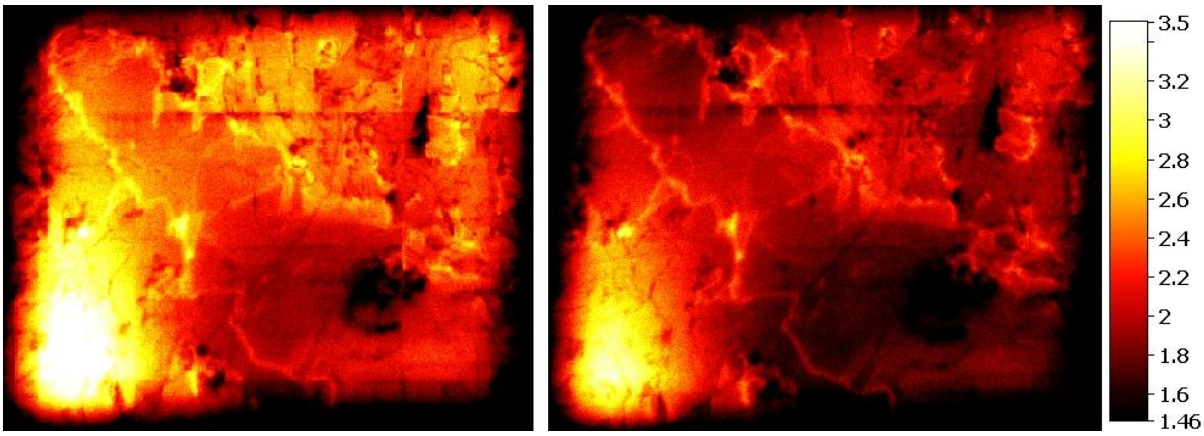


Figure 26: Calibrated images of wafer 3 before and after illuminating

The QSS-PC data gives the following values for the lifetime curves before and after. Δn is injection level in photons per cm³, τ is the carier lifetime in seconds.

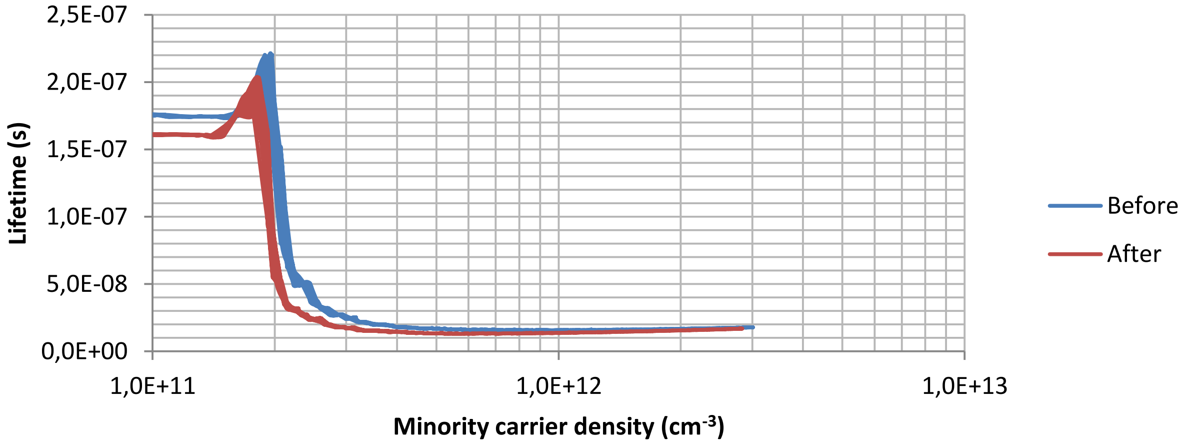


Figure 27: QSSPC before and after illumination of third wafer

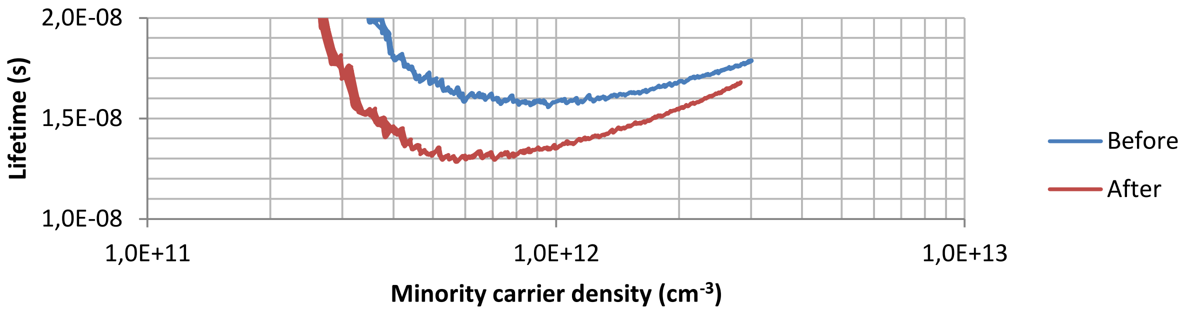


Figure 28: QSSPC before and after illumination of third wafer zoomed

When we zoom we see that there will probably be a cross-over point at an even higher injection level. However this cross-over point would not be in the region that is typical for iron-boron defects.

Fourth wafer
For the fourth measurement we used a wafer that has never been illuminated at 10 suns before, which means that the change on other defects is even higher. In the image we see a wafer with a high lifetime mostly in the left part. However it is hard to see a difference before and after illumination.

Before After

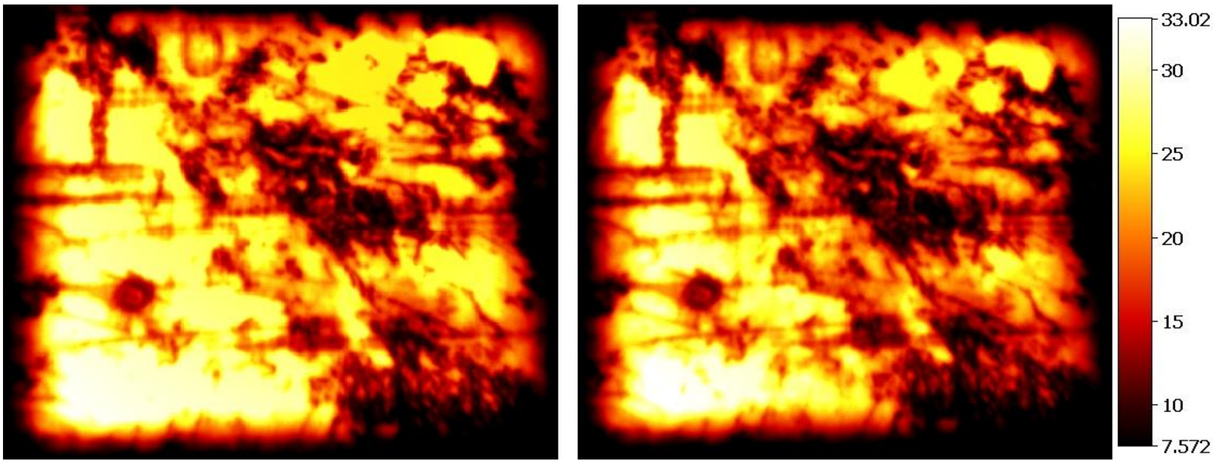


Figure 29: Calibrated images of wafer 4 before and after illuminating

The QSS-PC data gives the following values for the lifetime curves before and after. Δn is injection level in photons per cm³, τ is the carier lifetime in seconds.

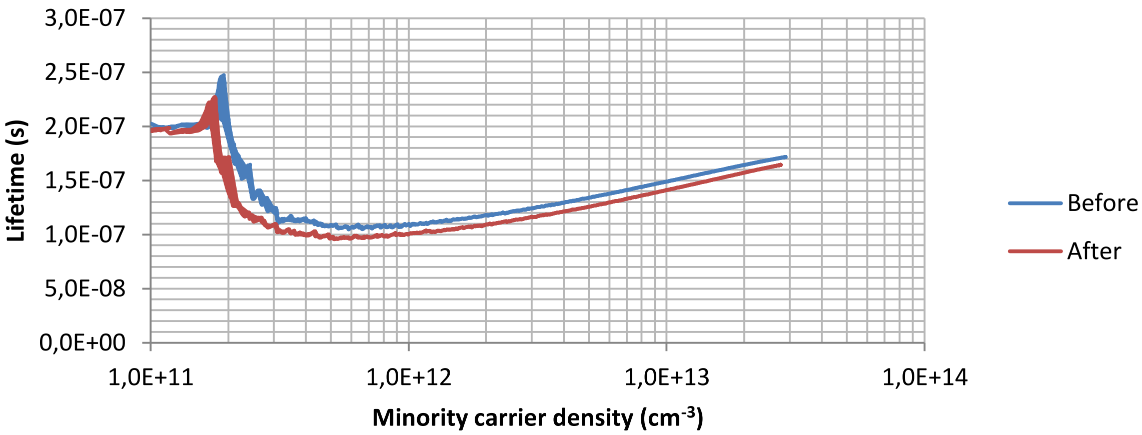


Figure 30: QSSPC before and after illumination of fourth wafer

From the QSS-PC curves we can see that there is barely any difference between before and after illumination. This wafer will not give a cross-over point.

Conclusion
In none of the wafers from this batch a cross-over point could be found. This probably means that there are other defects, most likely boron-oxygen, more dominant and therefore influencing the results. In the next test these defects have to be eliminated to find a cross-over point.

7.2 Test 2 – Finding cross-over point with PL laser; batch 2

Introduction

For this test a new batch of wafers will be used. In test 1 it became clear that if other defects are more dominant it is not possible to find a cross-over point. It has to be ensured that during this test boron-oxygen, the most likely other defect, does not play a role. To do this the wafers are first put under 1 sun illumination for at least 24 hours (Angelskar, 2011). This process will make sure that all boron-oxygen defects are split. After this the wafer will be placed in the dark for at least 12 hours (Macdonald, 2004), to ensure the FeB pairs that, split during the 1 sun illumination, are recombined. From here the wafers will be tested by the same procedure as in test 1 and a cross-over point might be found.

Samples

Not all specifications of the samples were given and therefore had to be determined.

Given

Doping: 4 n-type and 5 p-type multi-crystalline wafers.

Density: ρ = 2,3 gram / cm^3

Determined

Weight: 8,05 grams

Resistivity: 0,3 $\Omega \cdot cm$ on p-type
2.1 $\Omega \cdot cm$ on n-type
Resistivity is measured on no-passivated wafers from the same batch, because probes from the instrument can damage the passivation layer.

Calculated

Thickness: $d = \frac{W}{\rho \cdot A} = \frac{8,05}{2.3 * 12,4^2} \approx 221\ \mu m$

Procedure

The following steps has to be followed:

1. Place the wafer under 1 sun illumination source for at least 24 hours
2. Keep the wafer in the dark for at least 12 hours
3. Place wafer on calibration stage
4. Make QSS-PC lifetime curve and calibrated image
5. Change laser settings to; illumination area: small
   illumination time: 30 s
   photon flux (intensity): 4,23* 10^{18} cm^{-2} s^{-1}
6. Make an uncalibrated image 4 times (4 x 30 s = 2min) with the previous laser settings. The image will be useless but the purpose of this step is to expose the wafer to 10 suns for 2 min.
7. Change laser settings back to default
8. Make again a QSS-PC lifetime curve and a calibrated image
9. Compare images before and after and determine if lifetimes have a cross-over point in the expected region (around injection level of $2*10^{14}$)

Results
In the following lifetime images the lighter the area the higher the lifetime in this place.

P-type wafer
Figure 31 shows the lifetime image before and after 10 sun illumination. Both are after boron-oxygen splitting. We see no difference in lifetimes before and after.

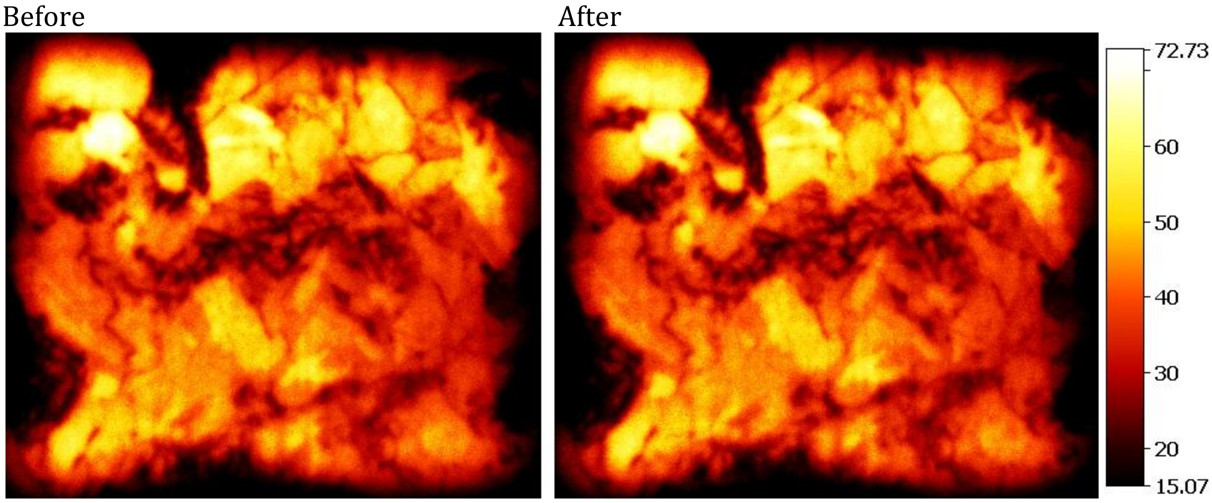


Figure 31: Calibrated images of p-type wafer before and after illumination

The curve in Figure 32 shows us that there was no cross-over point in the expected area. There is only a small difference measured before and after.

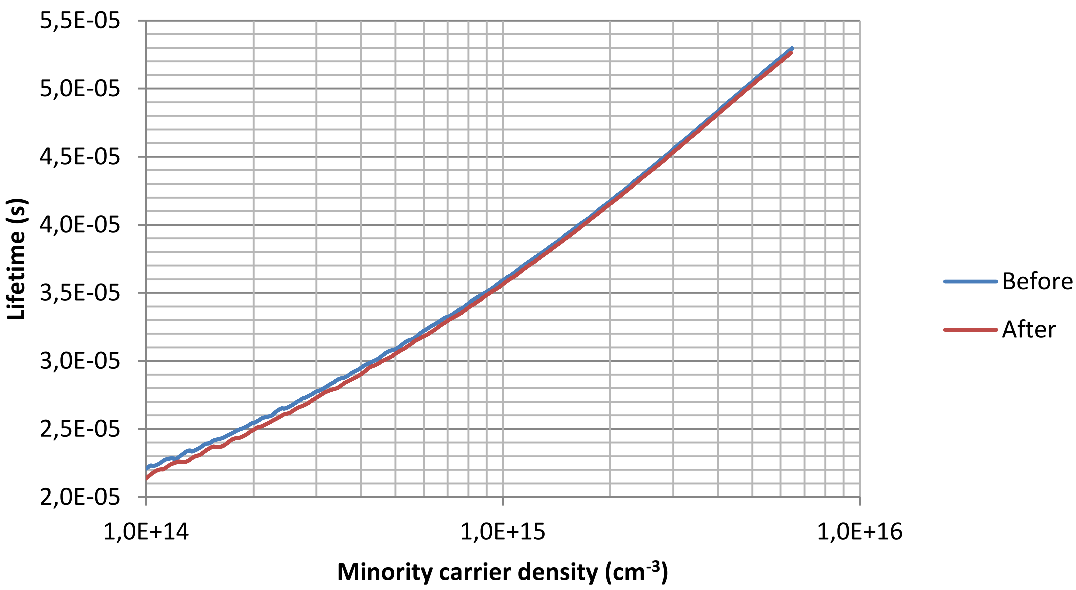


Figure 32: QSSPC curve p-type wafer

N-type wafer
Figure 33 shows the lifetime image before and after 10 sun illumination. Both are after boron-oxygen splitting. Barely any difference can be seen in these images.

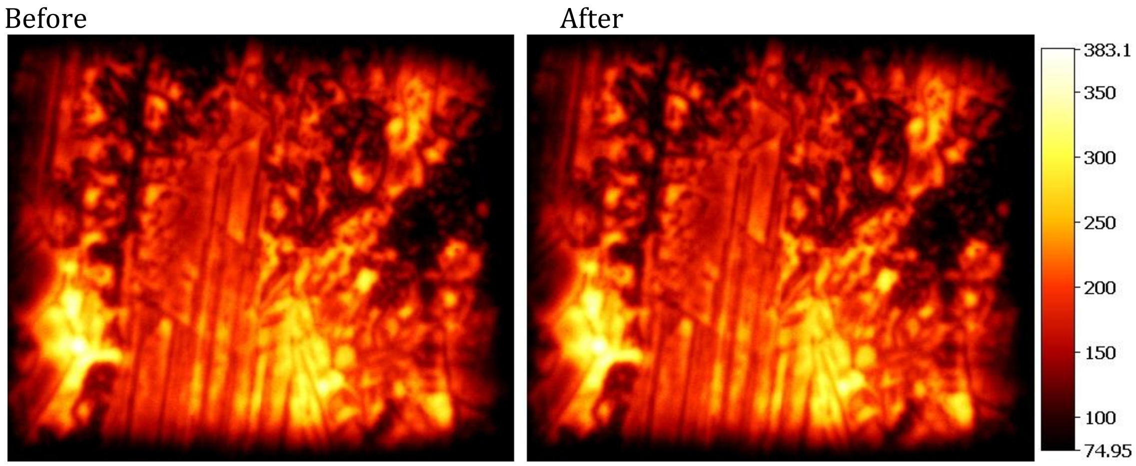


Figure 33: Calibrated images of n-type wafer before and after illumination

The QSSPC curve in Figure 34 shows the difference more clear. However the curves cross sometimes between $1{,}0*10^{14}$ and $1{,}3*10^{14}$ it cannot be counted as cross-over point since the 'after' curve should cross and stay above the 'before' curve.

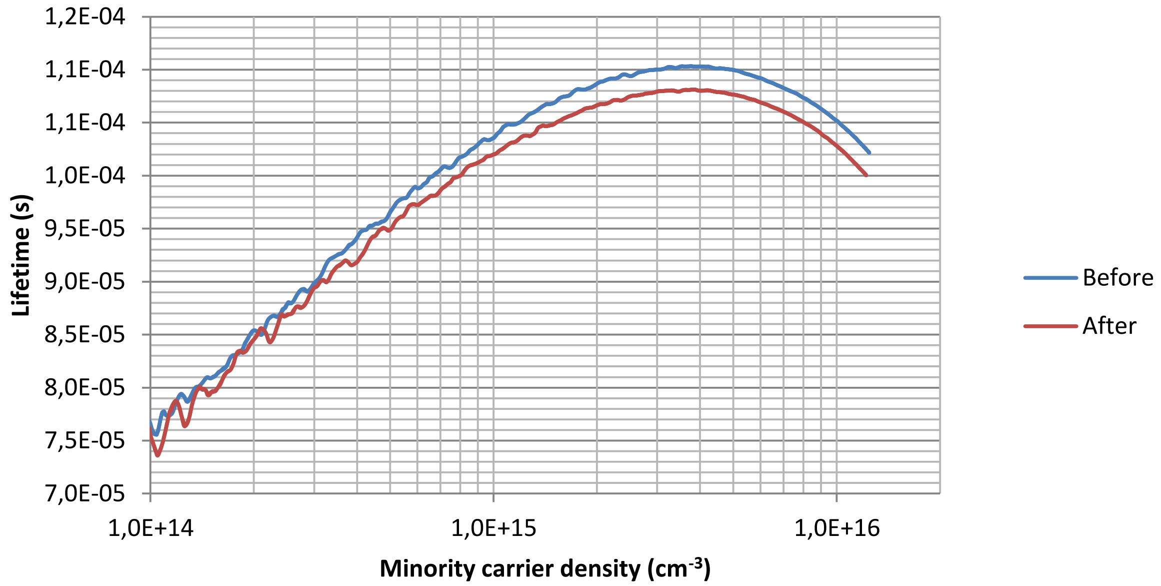


Figure 34: QSSPC curves n-type wafer

Conclusion

Despite the elimination of boron-oxygen defects, a cross-over point has not been found. Therefore we can say it is not possible to find a cross-over point by using the laser in the PL-setup on a small area of the wafer. Another option to get a cross-over point is to perform 10 sun illumination on a full wafer with an external light source (concept 6). This concept will be tested in test 3.

7.3 Test 3 – Finding cross-over point with external light source

Introduction
After finding out that it was not possible to make iron maps by only using the PL-setup, another option described in concept 6 (see chapter 5) will be tested. A flash head will be used for high intensity illumination. This light source is powerful enough to illuminate the entire wafer at 10 sun and so all iron-boron should theoretically be split. To test if building if building in a device like this in practice, the flash from another setup (μ-pcd) is used.

Figure 35: Flash head on μ-pcd

Procedure
1. Put wafer under 1 sun illumination for 24 hours to make sure all boron-oxigen complexes are split and will not influence iron measurements
2. Leave wafer in the dark for at least 12 hours to let the iron-boron pairs that are split during the 24 hour illumination recombine.
2. Make lifetime image and QSS-PC curve in PL-setup
3. Illuminate with 10 suns intensity with flash head (external light source)
4. Make again lifetime image and QSS-PC curve in PL-setup

Sample
The following specifications were given:

- Multicrystalline wafer
- Reflectivity: 32%
- Resistivity: 1.3703 $\Omega \cdot cm$
- Thickness: 170 μm
- Weight: 3,786 gram
- Doping: p-type

Results

The following lifetime images are made before and after illumination with the flash head:

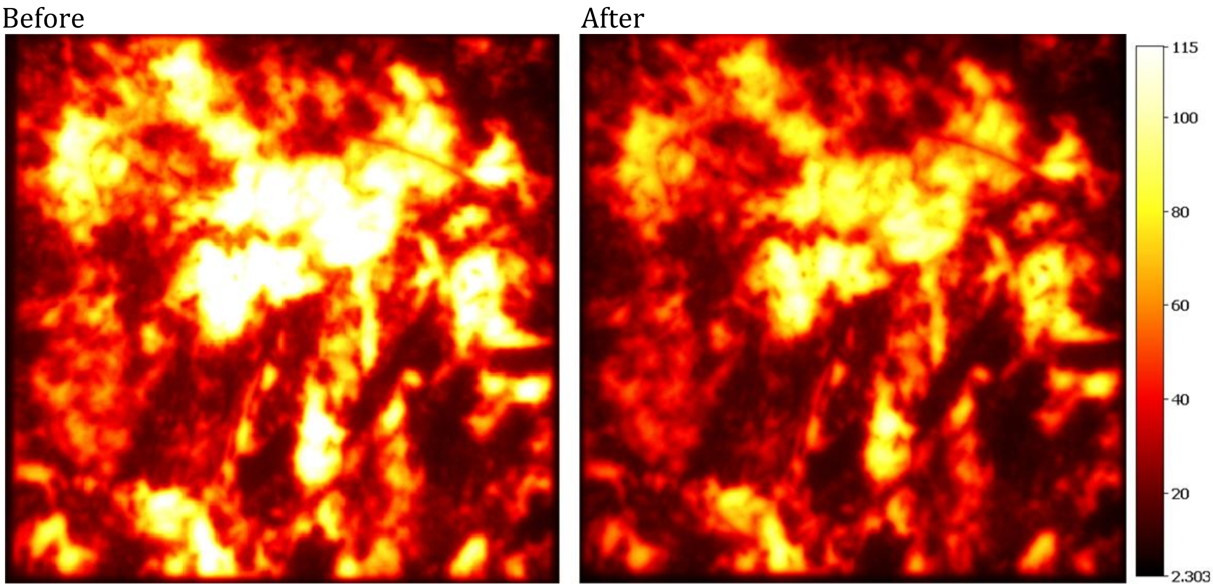


Figure 36: Lifetime images before and after high intesity illumination

The QSSPC curve in Figure 37 shows in fact a cross-over point in the correct region. The curve looks similar to the typical cross-over point curve so it can be assumed that images can be used to make an iron map.

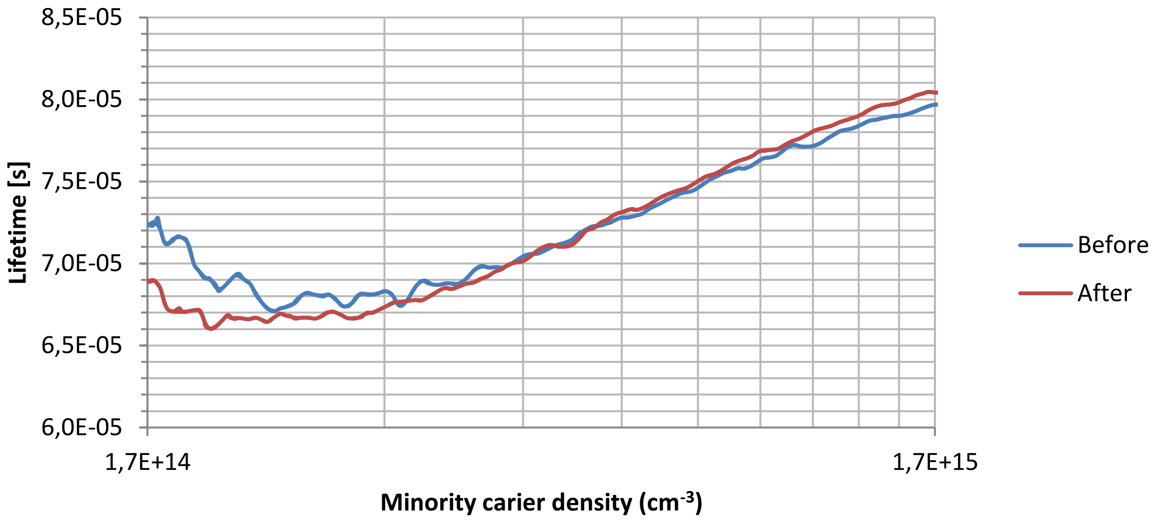


Figure 37: QSSPC curves of wafer illuminated by flash head

Conclusion

During this test a cross-over point was found after using a flash head to split the iron boron pairs. This means that the lifetime images made with this procedure can be used to make iron maps.

7.4 Test 4 – Hot plates; accuracy and homogenity

Introduction

Both old and new hot plates will be tested on accuracy and homogeneity by the use of a thermo camera. The camera has a resolution between 1 and 0,1°C. The maximum temperature that can be measured is 400 °C. The measured data can be used to get a better understanding about homogeneity and accuracy of both old and new hot plates.

Procedure

Wafers will be heated to different temperature set points and monitored by a thermo-camera.

Results

Old hot plates

Not all heat images are shown in this paragraph. However the results of all measurements are shown in Table 8.

Heat image at set point 50°C:

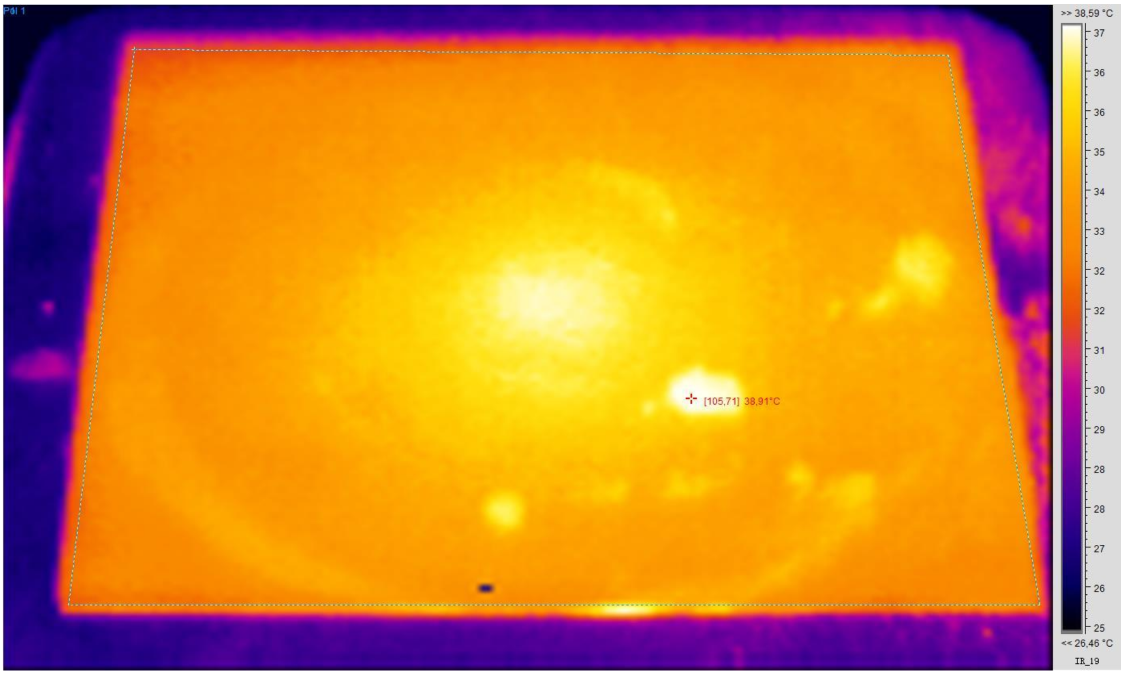


Figure 38: Heat image of wafer on old hot plate at 50°C

Set point [°C]	Average temp. [°C]	Max temp. [°C]	Min temp. [°C]
50	35,43	38.91	32.6

Table 5: Measurement data old hot plate setpoint 50 °C

Heat image at set point 150 °C:

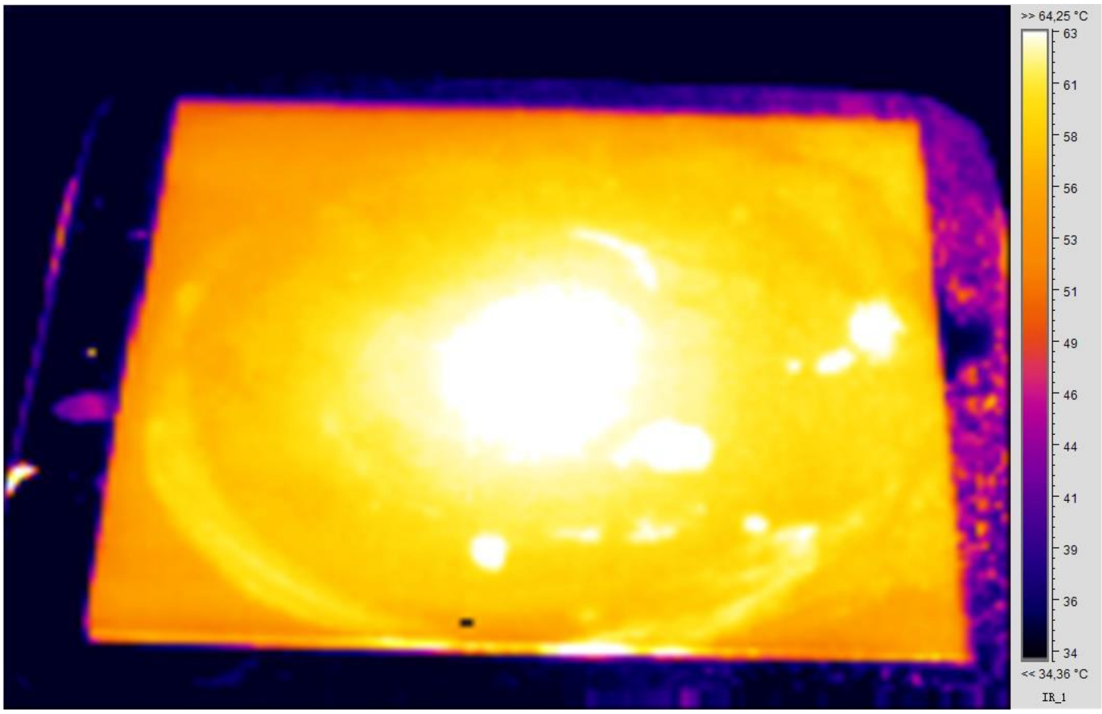


Figure 39: Heat image of wafer on old hot plate at 150°C

Set point [°C]	Average temp. [°C]	Max temp. [°C]	Min temp. [°C]
150	85,48	102,39	65,41

Table 6: Measurement data old hot plate setpoint 150 °C

Heat image at set point 250 °C:

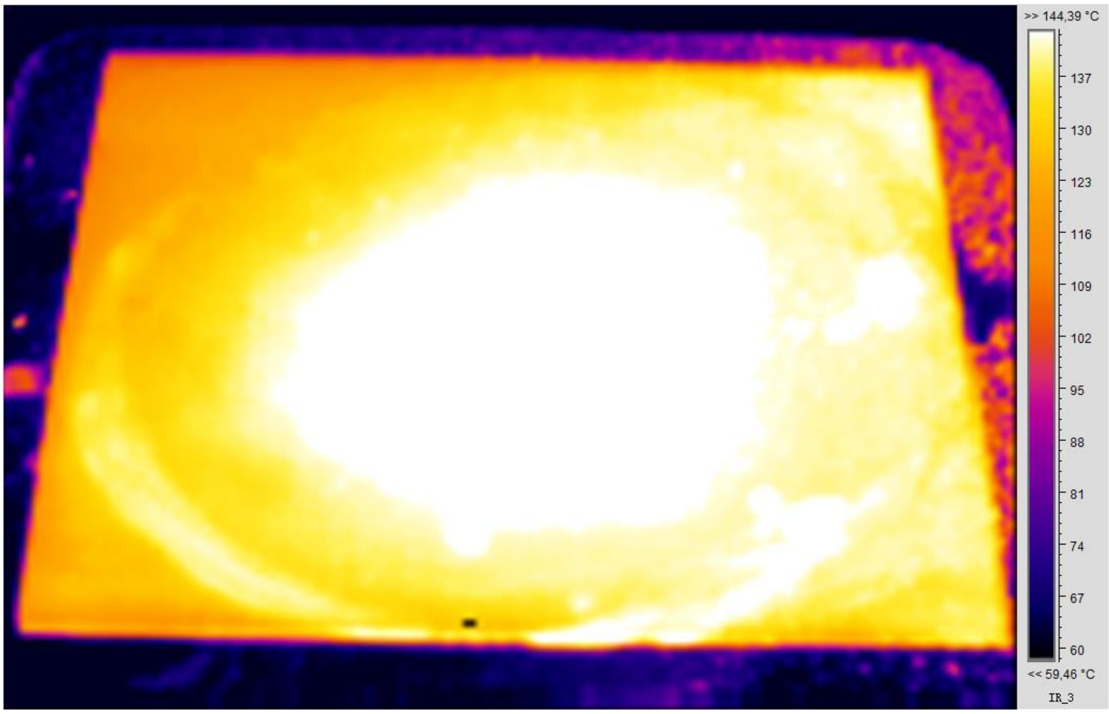


Figure 40: Heat image of wafer on old hot plate at 250°C

Set point [°C]	Average temp. [°C]	Max temp. [°C]	Min temp. [°C]
250	141,17	170,82	104,95

Table 7: Measurement data old hot plate setpoint 250 °C

The table below shows the measurement data of all set points:

Measurement #	Set point [°C]	Max. temp [°C]	Min. temp [°C]	Average temp [°C]
1	26	26,92	25,5	26,08
1	50	38,91	32,6	35,43
2	75	55,76	40,14	48,26
3	100	69,08	48,25	59,63
4	125	85,31	55,54	70,61
5	150	102,39	65,41	85,48
6	175	120,94	79,02	100,75
7	200	137,8	85,35	112,05
8	225	152,46	94,45	125,42
9	250	170,82	104,95	141,17

Table 8: Measurement data old hot plate all setpoints

Figure 41 shows the evolution of the maximum, minimum and average temperature as the set point temperature increases. As shown, even the maximum temperature never reaches the set point. The further the set point increases the bigger the deviation.

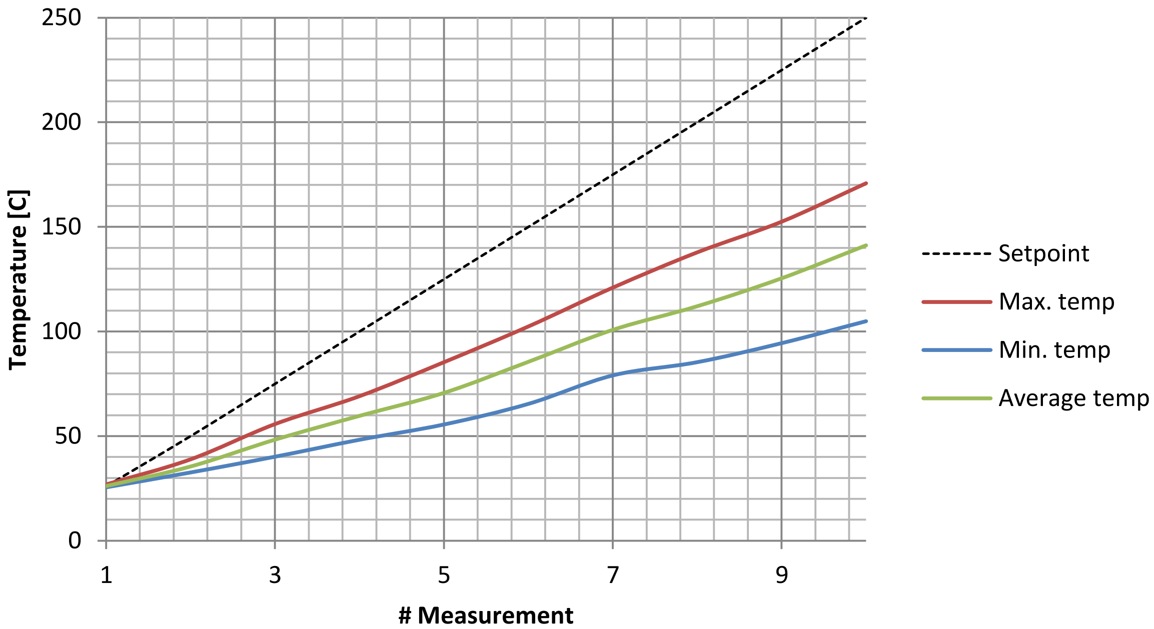


Figure 41: Evolution of maximum, minimum and average temperature of wafer on old hot plate

New hot plates
The same tests with the same wafer will now be performed on the new hot plates. All data is shown in table

Heat image at set point 50°C

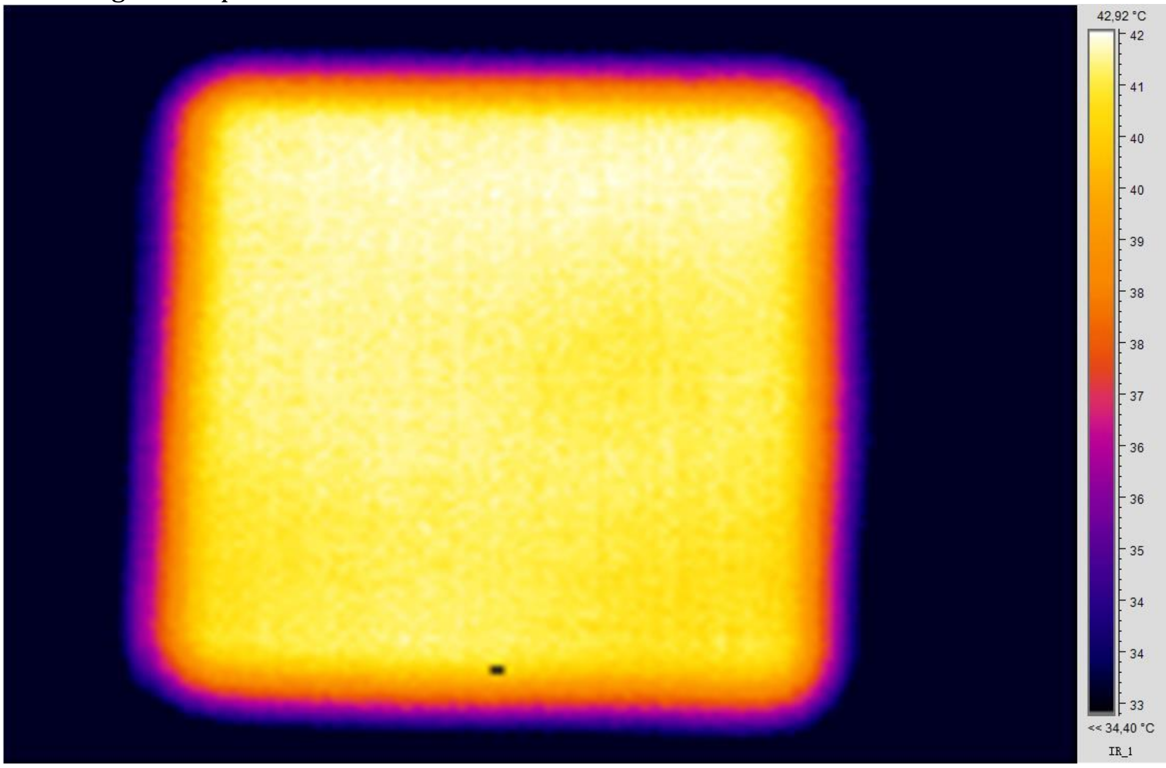


Figure 42: Heat image of wafer on new hot plate at 50°C

Set point [°C]	Average temp. [°C]	Max temp. [°C]	Min temp. [°C]
50	42,19	42,92	40,52

Table 9: Measurement data new hot plate setpoint 50°C

Heat image at set point 150°C

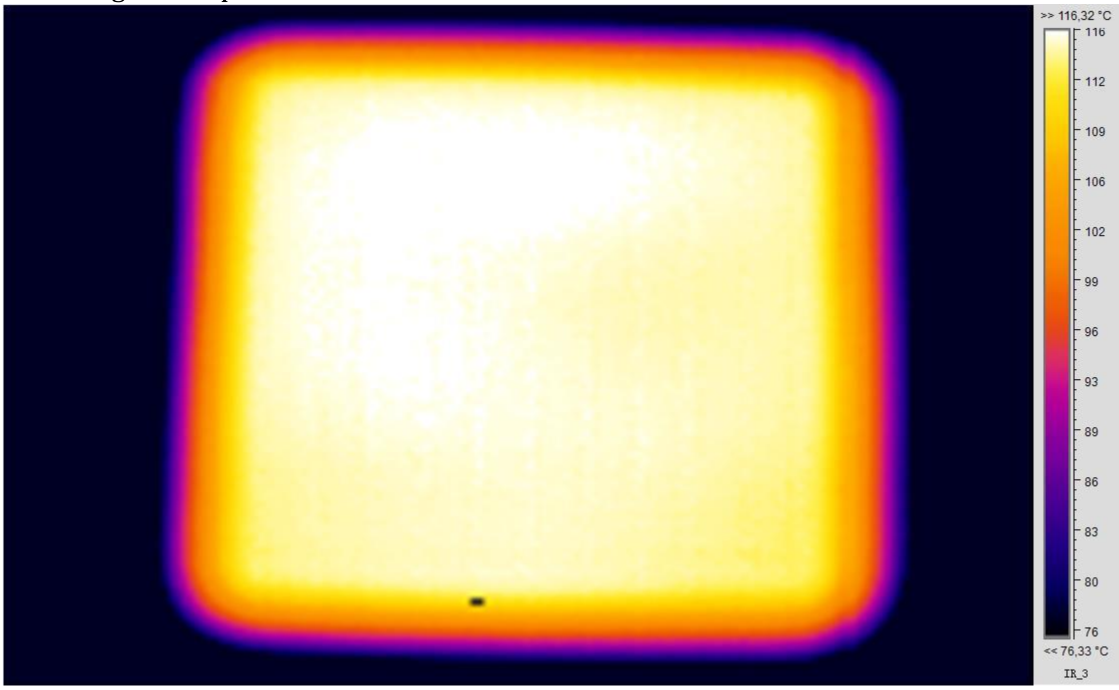


Figure 43: Heat image of wafer on new hot plate at 150°C

Set point [°C]	Average temp. [°C]	Max temp. [°C]	Min temp. [°C]
150	115,42	117,36	112,16

Table 10: Measurement data new hot plate setpoint 150°C

Heat image at set point 250 °C

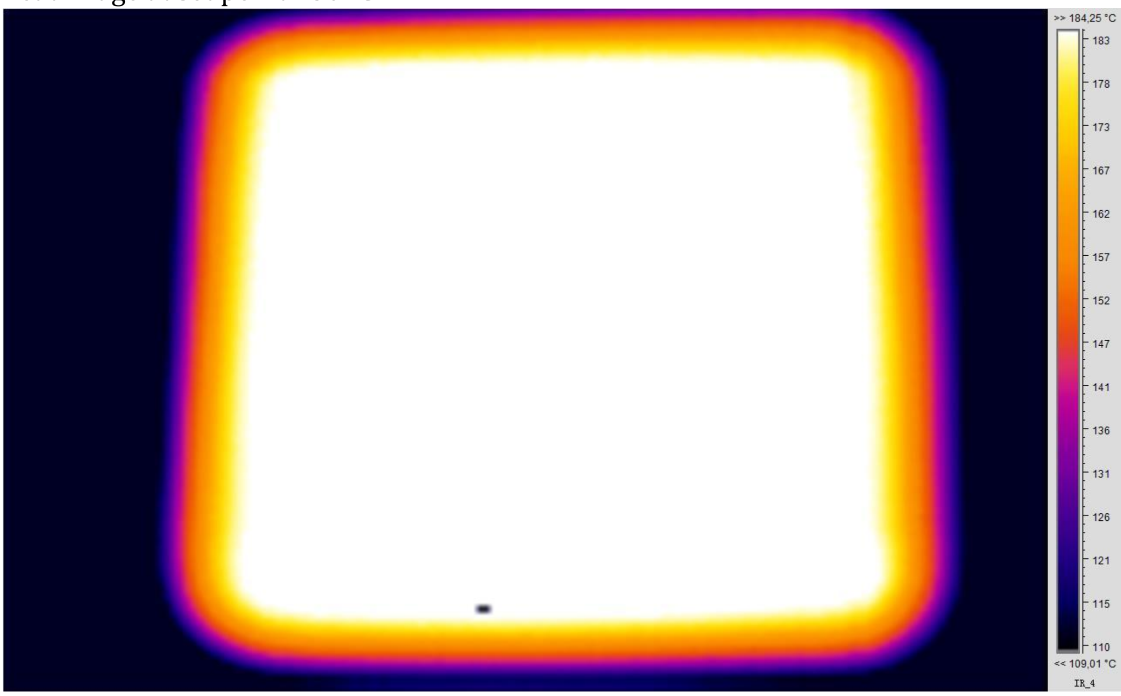


Figure 44: Heat image of wafer on new hot plate at 250°C

Set point [°C]	Average temp. [°C]	Max temp. [°C]	Min temp. [°C]
250	190,66	193,76	185,41

Table 11: Measurement data new hot plate setpoint 250°C

The table below shows the measurement data of all set points:

Measurement [#]	Set point [°C]	Max. temp [°C]	Min. temp [°C]	Average temp [°C]
1	24	24,62	23,46	23,92
2	50	42,92	40,52	42,19
3	75	62,08	59,47	61,12
4	100	81,28	76,06	79,78
5	125	98,2	94,41	96,81
6	150	117,36	112,16	115,42
7	175	142,05	131,88	138,5
8	200	156,17	148,36	153,48
9	225	176,17	163,84	172,68
10	250	193,76	185,41	190,66

Table 12: Measurement data old new plate all setpoints

This time we can see that the figure shows a much more homogenous heating process. The differences between the maximum and minimum temperature are small compared to the old hot plates. However, when the temperature of the hot plate increases the difference between the set point temperature and the average temperature increases.

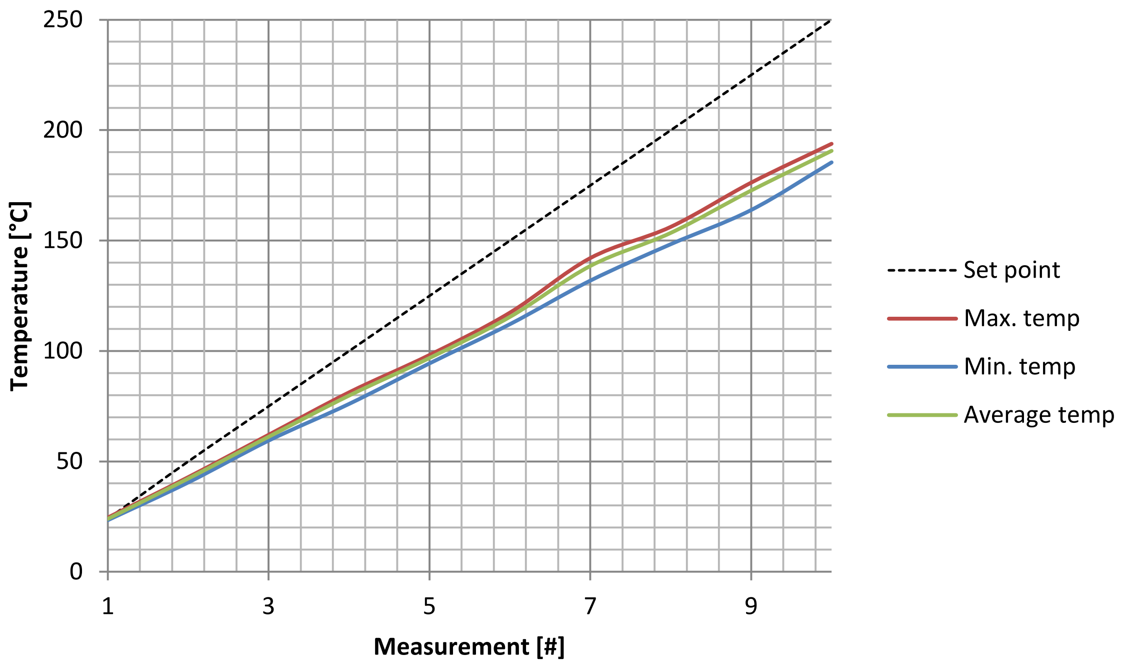


Figure 45: Evolution of maximum, minimum and average temperature of wafer on new hot plate

Homogeneity and accuracy
By looking at the deviation from the average temperature we can learn more about the homogeneity and accuracy of the hot plates. The tables below shows some calculated data of respectively the old and new hot plate.

Set point temp. [°C]	Average temp. [°C]	Max. deviation from average temp. [°C]	Average deviation from set point temp. [°C]
26	26,08	0,84	-0.08
50	35,43	3,48	14,57
75	48,26	8,12	26,74
100	59,63	11,38	40,37
125	70,61	15,07	54,39
150	85,48	20,07	64,52
175	100,75	21,73	74,25
200	112,42	26,70	87,95
225	125,42	30,97	99,58
250	141,17	36,22	108,83

Table 13: Homogeneity data old hot plate

Set point temp. [°C]	Average temp. [°C]	Max. deviation from average temp. [°C]	Average deviation from set point temp. [°C]
24	23,92	0,70	0,08
50	42,19	1,67	7,81
75	61,12	1,65	13,88
100	79,78	3,72	20,22
125	96,81	2,40	28,19
150	115,42	3,26	34,58
175	138,50	6,62	36,50
200	153,48	5,12	46,52
225	172,68	8,84	52,32
250	190,66	5,25	59,34

Table 14: Homogeneity data new hot plate

The figure below compares the maximum deviation from the average temperature of both hot plates. We can see that the new hot plate increases much slower than the old one and which means that it heats the wafers significantly more homogeneous.

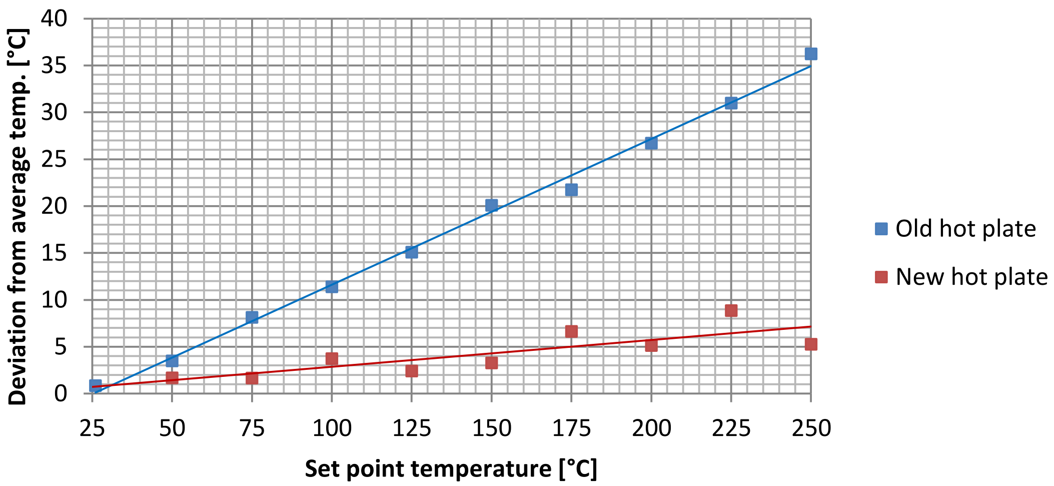


Figure 46: Maximum deviation in temp. of both hot plates

The following figure shows average deviation from the set point temperature. By looking at these values we can see how accurate the hot plate is. The larger the gradient of the curve, the lower the accuracy of the hot plate.

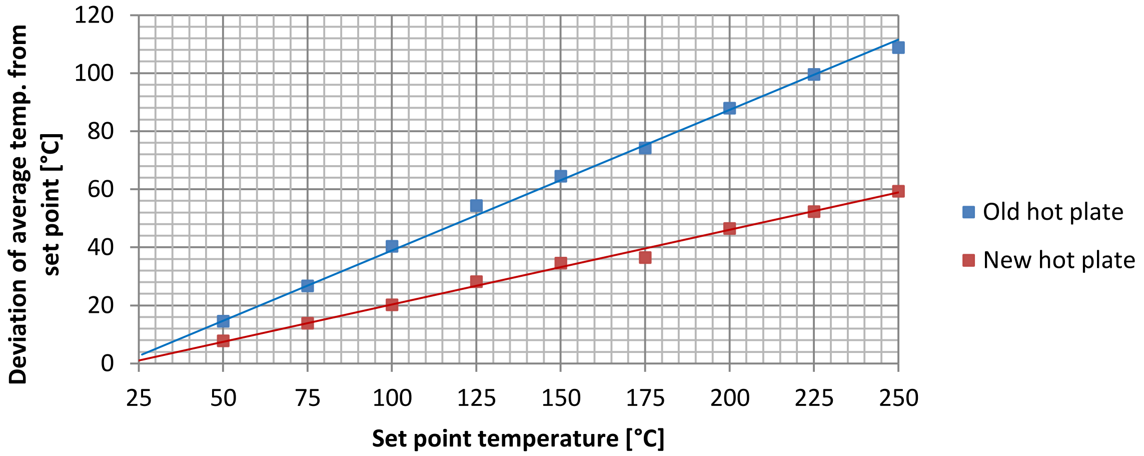


Figure 47: Deviation of average temp. from set point of both hot plates

Conclusion and discussion

Figure 46 shows a clear difference in deviation. The curve of the old hot plate increases strongly. The same is shown in Figure 41 where a larger variation between maximum, minimum and average temperature can be seen as the set point temperature increases. This means there is a low homogeneity, which is also proved by the heat images (Figure 38, Figure 39 and Figure 40). For example at set point 150 °C there is a deviation of up to 23,5% from the average temperature. At set point 250 °C the maximum deviation from the average temperature is even 25,7%. This kind of temperature differences inside the wafer make them useless for research.

The new hot plate shows a different behavior. Figure 46 shows a much slower increase and the maximum, minimum and average temperature don't vary much. This is also proven by the heat images which show a much more homogenous plate (Figure 42- Figure 44). If we make the same calculations as with the old hot plate we see that the maximum deviation of the average temperature at set point 150 °C is 2,8%, whereas for set point 250 °C the same deviation of 2,8% is found. This high homogeneity makes the new hot plate meet the requirements for research purposes.

Nevertheless in both cases we see that the actual temperature differs significantly from the set point temperature (Figure 47). This might be due to poor contact between the wafer and the hot plate surface. In case of the old hot plates it is visible that the plate is not completely flat, which can also be seen by looking at the heat distribution in the heat images. However, the new hot plate has a flatness of 0,127mm, so it is unlikely to be the cause of deviation. It has to be mentioned that during the test the vacuum channels could not be used, so it can be assumed that differences will be significantly lower if a vacuum pump is connected to suck the wafer to the plate. For this reason it is recommended to always use the heat camera to monitor the actual temperature of the wafer.

7.5 Test 5 – Hot plates; influence of heat on lifetime

Introduction

To test the heating stage in the PL-setup, lifetime measurements will be done at a p-type wafer at different temperatures up to 100 °C. In the results we expect to see lifetime being dependent on temperature.

Procedure

During this test the following procedure has been followed:

1. Make uncalibrated image of the wafer on calibration stage
2. Install heat stage
3. Make uncalibrated images at different temperatures

Sample

Same batch as test 2 (see 7.2 for calculations).

Doping:	p-type multi-crystalline wafer
Weight:	8,05 grams
Resistivity:	0,3 $\Omega \cdot cm$ on p-type
	2.1 $\Omega \cdot cm$ on n-type
Thickness:	221 μm

Results

The image below shows an uncalibrated image of the wafer on the calibration stage before heating on the heating stage.

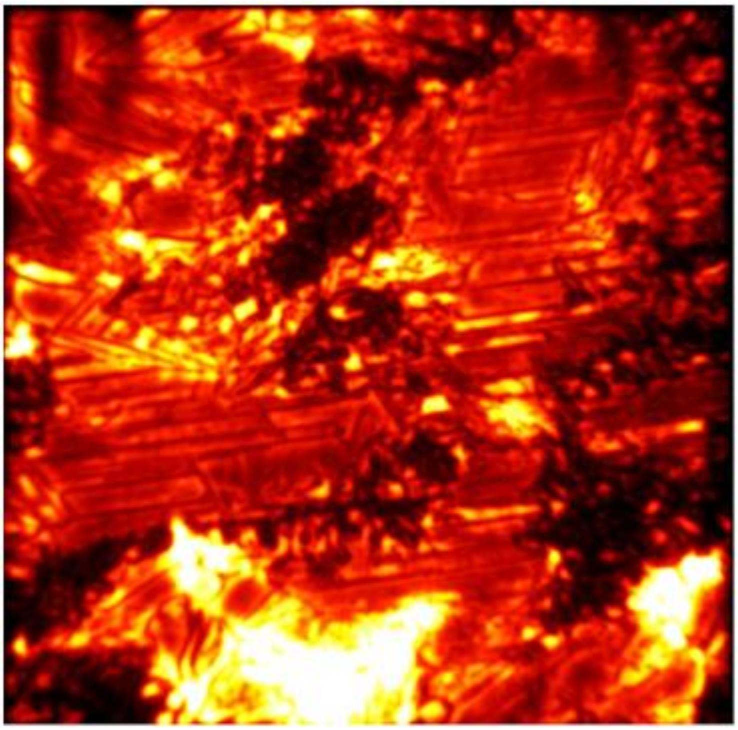


Figure 48: Uncalibrated imaged on calibration stage

The figure below shows the uncalibrated images at different temperatures on the heating stage. Every image has the same scale. There is no numbered scale shown since the images are not calibrated so there are no relative values for the lifetimes. The colors in the images can be used for lifetime comparison. The lighter the color the higher the lifetimes.

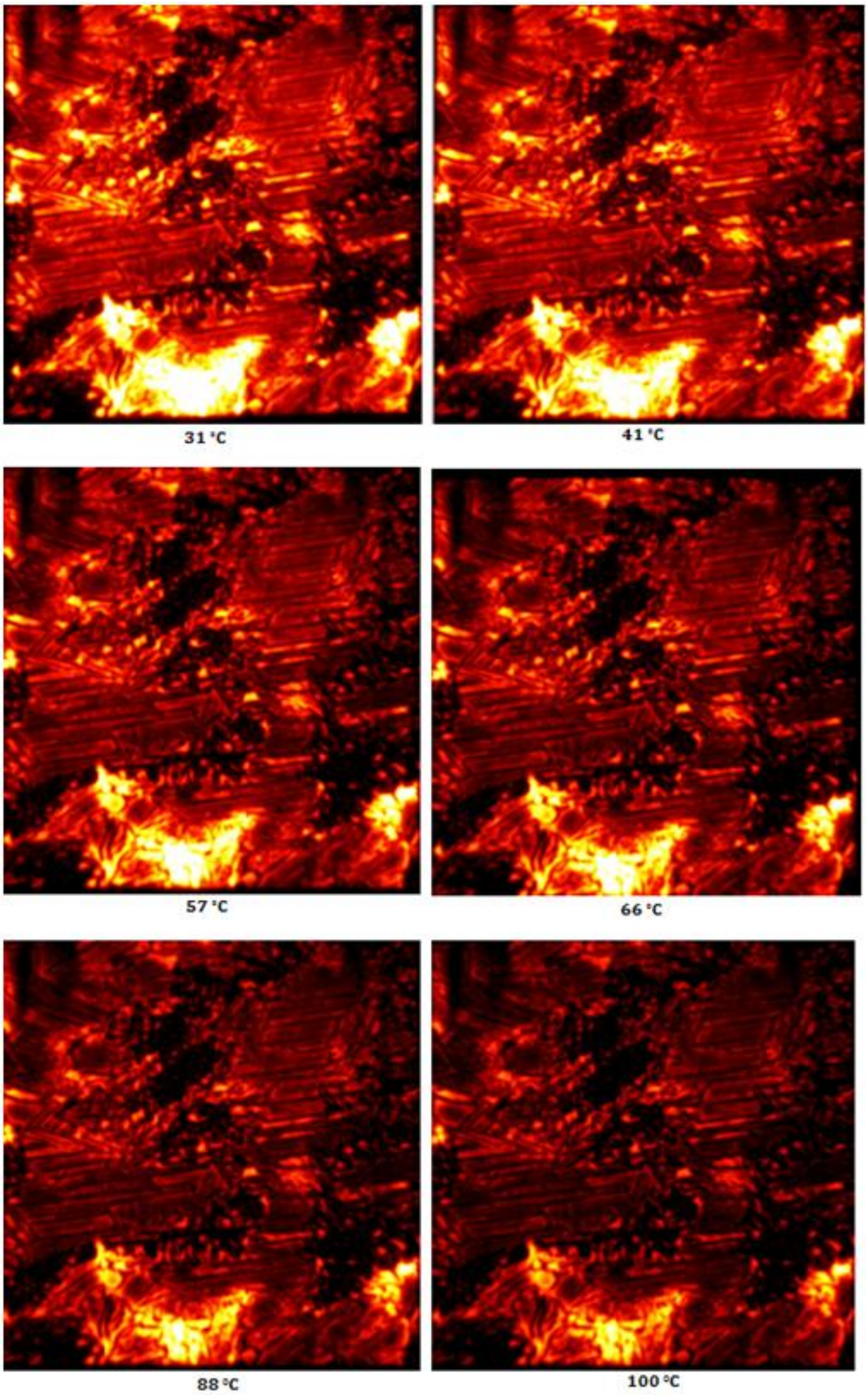


Figure 49: Uncalibrated images of wafer at different temperatures

Conclusion

As expected the lifetime of multi-crystalline silicon wafers is dependent on the temperature. The results show that the heating stage fulfills the requirements and makes clear images. The heating stage can now be used for other research.

8 Conclusion and recommendations

In this chapter an overall conclusion will be drawn from all the tests in chapter 7. Furthermore some recommendations will be given for the people who will continue this work or use the equipment.

Iron mapping
The first three tests have shown that it is not possible to find a cross-over point by focusing the laser in the PL-setup. It is however possible to reach a cross-over point when an external light source is used to illuminate the full wafer. Due to lack of specifications the photon flux of the two light sources cannot be compared, but in theory the laser should also be powerful enough for iron-boron splitting. The fact that with the laser only a small part is illuminated should also not play a role. In this small area, all the iron-boron pairs should be split and only this part is looked at by the CCD camera. An explanation might be that the camera is not precisely focused above the coil and therefore the QSSPC coil, which is used to make the lifetime curves, displays the lifetimes of areas that were not illuminated. This might also explain why a cross-over point could be found when the wafers were fully illuminated. In this case the coil can be placed under every point of the wafer without influencing the results.

To overcome this problem the camera should be focused properly, preferably by the manufacturer. Afterwards test 2 should be repeated. If then it is still not possible to find a cross-over point, one can be sure that the PL-laser cannot be used for iron mapping. In this case it is recommended to use an external light source. The possibility to build this light source into the PL-setup should be further examined since the extreme temperature might harm the electronics in the PL-setup.

Heating stage
Test 4 and 5 have shown results on the implemented heating stage. Most of the requirements stated in chapter 4 were met. The down time of the PL-setup during implementation of the stage did not influence other research projects. Furthermore, the stage can be removed easily and no permanent changes had to be made on the PL. Test 4 shows that in terms of homogeneous heating of the wafer, a large improvement is made on the old hot plate. Unfortunately the requirement of only 1.0°C deviation could not be met at high temperatures, therefore the deviation should be taken into account when measurements are done at higher temperatures. The accuracy of the new hot plate was also an improvement compared to the old hot plate, but in test 4 one can still see quite large differences between set point and actual temperature. An explanation for this is that the vacuum channels could not be used during this test. The hot plate is expected to be more accurate when these channels are used and therefore it is recommended to repeat test 4 with the use of the vacuum channels.

Test 5 shows that the heating stage can be successfully used in the PL-setup. Clear images could be obtained and the results show a temperature depended behavior of the multi-crystalline wafers. This gives various opportunities for new research.

9 Future work

The features which are implemented in the photoluminescence setup during this thesis enable scientists at IFE to do new research. Following is a list of new areas that can be researched because of this thesis work:

- The heating stage will be used to do lifetime measurements at different temperatures. Currently lifetime measurements in the solar cell community, including all the measurements in the PL-setup are done at room temperature. In reality however, solar cells usually operate at higher temperatures (up to 80°C). The new stage will give the opportunity to test the wafers at conditions similar to in the field.

- The possibility to heat the wafers up to 375°C gives opportunities for new research at fundamental level. By changing the temperature variable it will be possible to expose the nature of different defects in the silicon wafers. This will allow researchers to pinpoint which defect structures at atomic levels are responsible for efficiency losses, and to use this information to develop better solar cell silicon materials.

- The ability to make iron maps with the PL-setup will be further examined. After implementing a successful method, either with a flash head or by using the laser, iron maps of silicon wafers can be made by the PL. These maps of single wafers will finally be used to make 3D iron maps of an entire block, which are invaluable for further silicon production process optimization.

List of figures

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Attachment I – Hot plate manufacturers

Company	Product	Heating	Cooling	Vacuum	Temp. Range [°C]	Temp. Regulatio	Made in	Link
Wenesco Inc.	HP662	x	x	x	0 -400	Ditigtal	USA	http://ww
Elkom	Custom	x	x				Germany	http://ww
Busse	Custom	x	x		0 -300	Digital	Germany	http://ww